# A High Resolution First Order Noise-Shaping Vernier Time-to-Digital Converter

**Majid Memarian Sorkhabi[*], Siroos Toofan**

[1]Department of Electric Engineering Zanjan University, Iran
*Corresponding author: Memarian@znu.ac.ir

**Abstract**  In this paper, we propose a noise reduction method for a Vernier Time-to-Digital Converter (VTDC) using a first-order noise shaping structure and a gated ring oscillator (GRO). An 11bit VTDC with 4 p s effective resolution was designed and developed for a high performance All Digital Frequency Synthesizer (ADFS). The VTDC realized in 180nm CMOS, its power consumption depending on the time difference between input edges; 1 to 11mA from a 1.5 V supply.

## 1. Introduction

Wireless communication has grown exponentially, with wide range of applications offered for the customers. Among these, WLAN (2.4-2.5GHz, 3.6-3.7GHz and 4.915-5.825GHz), Bluetooth (2.4 GHz), and WIMAX (2.500-2.696 GHz, 3.4-3.8 GHz and 5.725-5.850 GHz) communication standards have found largest use local area, indoor – outdoor communication and entertainment system applications.

As technology has advanced, on-chip clock multiplication has become a necessity for nearly all digital integrated circuits (ICs) and wireless standards instead of realize high speed clock signals from lower speed external sources such as crystal oscillators. The typical approach to achieve such clock multiplication is to employ a phase locked loop (PLL) circuit consisting of a phase detector, analog loop filter, frequency divider, and Voltage-Controlled Oscillator (VCO). Unfortunately, the analog component of PLLs prevents their design from simple compatibility with a typical digital design low [1].

Among various digitally-assisted analog techniques, the All Digital frequency synthesizer (ADFS) has especially become a very hot research topic in the past few years after it was demonstrated to be able to proper the stringent wireless communication requirements and specifications [2].

The Time-to-Digital Convertor (TDC) is a fundamental block in the ADFS that can bridge the gap between the continuous-time analog domain and the discrete-time digital domain. Achieving high performance in such systems associates on their TDC performance, which is used to measure the instantaneous time difference between the edges of PLL output and an input reference clock [3].

The noise performance of a synthesizer is most often characterized by phase noise, which is a measure of the spectral purity of the system output. This topic has been extensively studied in literature and is an active area of research [3,4]. It is known that all synthesizers exhibit phase noise. This phenomenon degrades signal transmission quality by allowing noise at other frequencies to fold into the band of interest. The significant point is that reduction of phase noise for increasing transmission rates while keeping bit-error rates tolerable and acceptable [4].

Motivated by the above goals, a low noise high performance Vernier TDC (VTDC) for wireless communication which is highly integrated in digital standard cells is presented in this paper. An 11bit VTDC with 4ps effective resolution was designed and developed for a high performance ADFS.

Due to TDC finite resolution, a TDC introduces quantization noise on the output of ADFS spectrum. Several techniques have been proposed in the literature to enhance the resolution of TDCs and to reduce the quantization noise like noise shaping [3,5].

In the noise shaping TDCs, the resolution and signal to noise ratio at low frequencies are improved by pushing the power of the quantization noise to high frequencies.

Since the loop filter within the PLL acts to filter out the high frequency noise produced by the noise shaping, noise shaping yields greatly improved effective resolution of the TDC characteristic.

## 2. Background

An Figure 1 expresses two type of ring oscillator-based TDC. First of all we consider a classical architecture of TDC.

### 2.1. Classical Architecture of TDC

As shown in Figure 1(a), the classical ring oscillator-based TDC composed of a ring of delay elements [3]. First, the oscillator transitions are counted during the input time window Tin here indicated by the Enable signal.

This topology works by counting the number of sequential inverter delays that occur during the Enable signal. To explain its operation, the rising edge of the start signal, which represents the first event, is sequentially delayed by a series of inverter gates, each with delay Tq, The output from one of these inverters is an input for a counter. It is counted rising or falling edge, until the rising edge of the stop signal, representing the second event, is occurred. The TDC output code is then generated at the register output, which corresponds to the number of delay elements that have transitioned within the measurement interval (Tin) and has been counted by counter. The counter resets the value when the Enable signal is low.
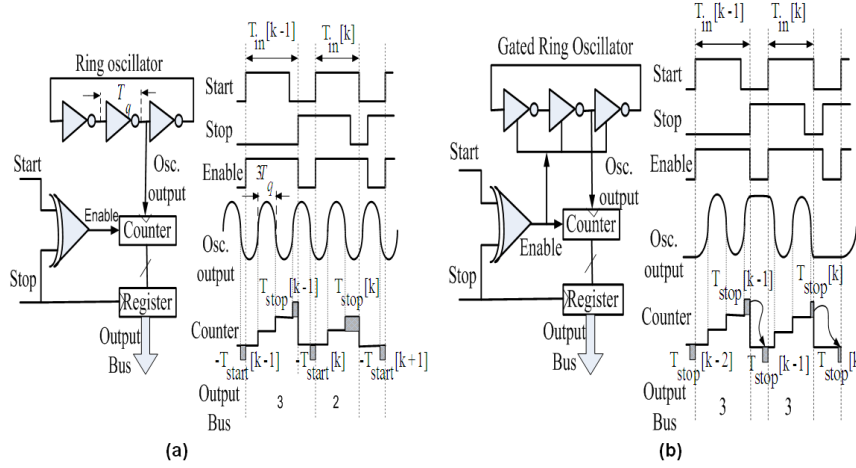


**Figure 1.** Ring oscillator-based TDC (a) Classical architecture, (b) With noise shaping architecture

We find that counting the transitions of a free running oscillator results in error equivalent to the fundamental expression is given by:

$$\text{Terror}[k] = \text{Tstop}[k] - \text{Tstart}[k] \quad (1)$$

Let the Tstart and Tstop denote the times at the beginning and end of the Enable signal. There is an error to this method at both the beginning and end of the measurement, which indicates that each measurement of the ring oscillator-based TDC will have an additional error contribution from Tstart.

### 2.2. Noise Shaping Architecture of TDC

Figure 1(b) illustrates the concept of a noise shaping architecture of TDC, which is similar to the previous ring oscillator-based TDC. Like that method it measures the number of delay element transitions during a measurement interval.

However, the key innovation in the noise shaping method is that instead of enabling the counters during the measurement window, the ring oscillator itself is gated with the Enable signal, with the state of the oscillator preserved in between measurements. By preserving the oscillator state at the end of the measurement interval Tin[k-1], the quantization error Tstop[k−1] from that measurement is also preserved. In fact, when the following measurement of Tin[k] is started, the previous quantization error is carried over as Tstart[k] = Tstop[k−1]. This results in first-order noise shaping of the quantization error in the frequency domain, as evidenced by the first-order difference operation on Tstop. Therefore the measurement error is given by:

$$\text{Tstar}[k] = \text{Tstop}[k-1] \quad (2)$$

$$\text{Terror}[k] = \text{Tstop}[k] - \text{Tstart}[k] \quad (3)$$

Thus

$$\text{Terror}[k] = \text{Tstop}[k] - \text{Tstop}[k-1] \quad (4)$$

$$\text{Terror}[k] = \left(1 - z^{-1}\right) \text{Tstop}[k] \quad (5)$$

Because the next quantization error is subtracted from the previous one, equation (4) corresponds with a first-order noise shaping in the frequency domain.

## 3. The Vernier TDC

As shown in Figure 2, two rings of inverters with slightly different delays (Tslow, Tfast) are used to digitalize the difference of time interval between reference clock and feedback clock which triggers the enable signals.
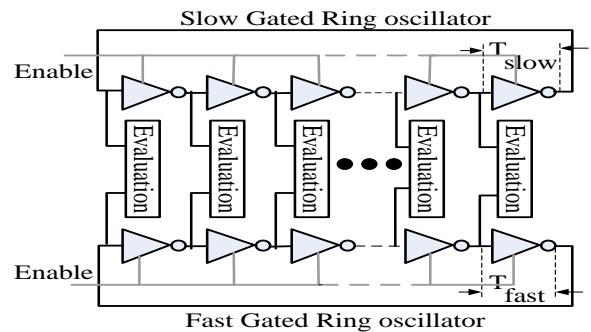


**Figure 2.** Vernier TDC

When the enable signal of slow ring is asserted, slow GRO starts to oscillate, and the number of oscillations is counted by a coarse counter. Then, after an input delay of Tinput, the enable signal of fast ring triggers the faster GRO Instantaneously, at this moment, the coarse counter is disabled. To improve the measurement accuracy, the residue of the input delay is measured by the Vernier structure.

Since Tfast is smaller than Tslow, the time difference between rising edges of two oscillations is reduced every cycle by the difference in periods (Tslow – Tfast), and the

edge of the fast GRO eventually catches up with the slow GRO. The arbiter circuits have deduced this catches up. By counting the number of cycles it takes for the fast GRO to catches up with the slow GRO, time interval can be determined (Tinput).
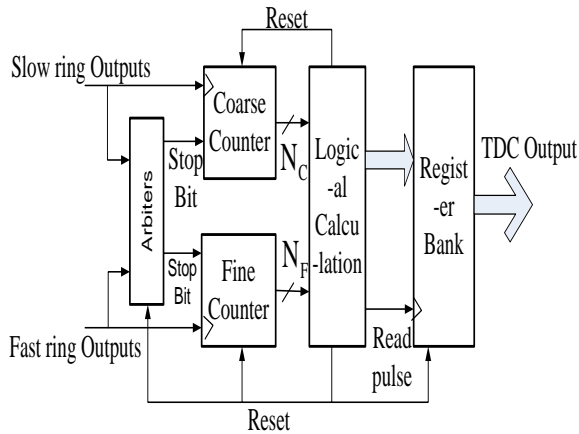
# 4. Evaluation Logic



**Figure 3.** Evaluation block diagram

Evaluation block was depicted in Figure 3. First of all, rising edges and falling edges of slow and fast GRO fed into arbiters. The two types of arbiters are placed alternatively along the rings to compare the rising or falling edges, respectively. An arbiter judges whether the reference leads the feedback or vice versa.
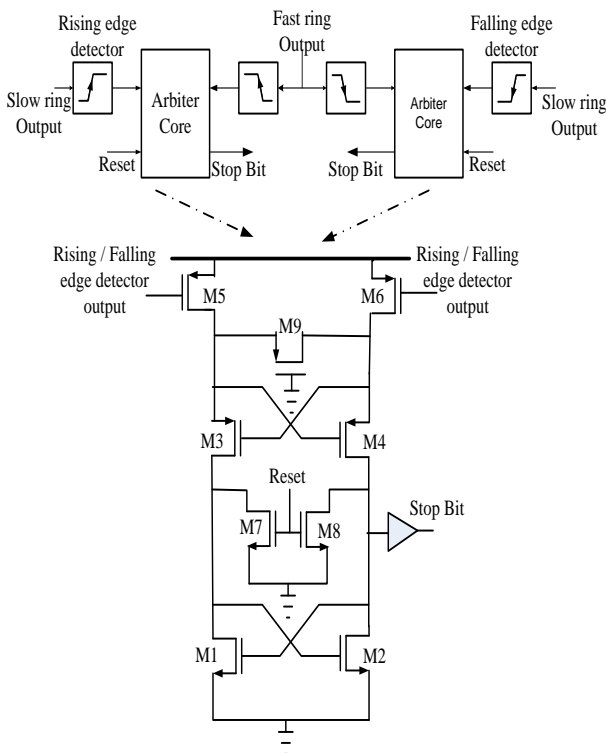


**Figure 4.** Circuits of arbiters

The output bit of Arbiters controls the fine and coarse counters which were identified as stop bit in Figure 3.

Figure 4 describes the schematics of proposed arbiters used in the VTDC [6]. The arbiters need to be reset at each judge before the next comparison starts, so reset

circuit is utilized in an arbiter core. Rising and falling edge detectors are shown in Figure 5.
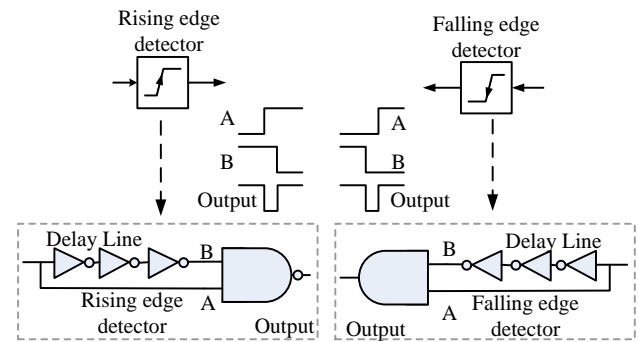


**Figure 5.** Rising and falling edge detectors

Eventually Calculation logic in the Evaluation black combines the fine and coarse counters outputs for an estimation of the time interval and sends it for register bank. This bank exported the calculated digital words when had triggered with the read pulse.

# 5. Simulation Results

The proposed VTDC was simulated by RF-H spice software with 180nm RF-CMOS technology. The simulations were carried out using a F Ref = 40MHz reference clock.

The power consumption of the VTDC is a linear function of the width of the enable signal, corresponding to its input. Simulation results show at 1.5 V supply, the power ranges from 1.5mW to 16.5mW. Since higher supply voltage arrives to a shorter delay per delay stage, we will present simulation results at 1.5 V in order to find the best practical performance of the GRO. At this voltage setting, the time resolution of the proposed VTDC (bin size or 1 LSB) is 4 ps. This result verifies the significant benefit in time resolution.

The achieved resolution of 4ps represents an improvement factor of over 7 compared to a classical TDC resolution of 30–35ps under the same voltage supply and operating conditions [7].

Figure 6 shows the time domain VTDC output code with a 100 kHz input of 2pspp and 40MHz reference, in addition to a dc level of about 1ns.
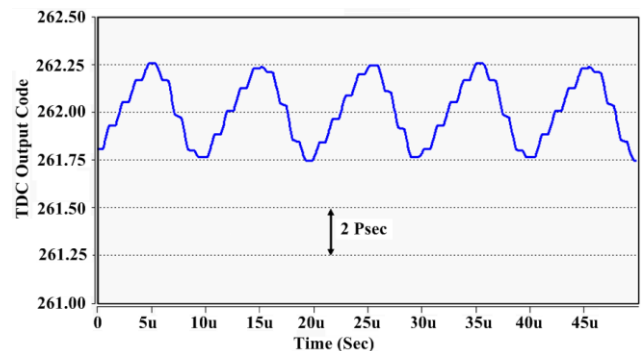


**Figure 6.** VTDC output with sinusoidal delay sweep 2 p s (p-p)

Figure 7 and Figure 8 display the simulated power spectrum of the VTDC output corresponding to the conditions as just mentioned. For best compare between VTDC with noise shaping and without noise shaping,

Figure 7 expresses the classical VTDC while noise shaping was disabled.

For a classic vernier TDC which has not noise shaping, the quantization noise has a "white" noise floor (as shown in Figure 7). However in the proposed VTDC, most of the quantization noise is pushed to high-frequency region (first-order shaped). Noise shaping of more than 10dB is clearly apparent and the simulated results have very good agreement with the theoretical first-order noise-shaping (as shown in Figure 8).
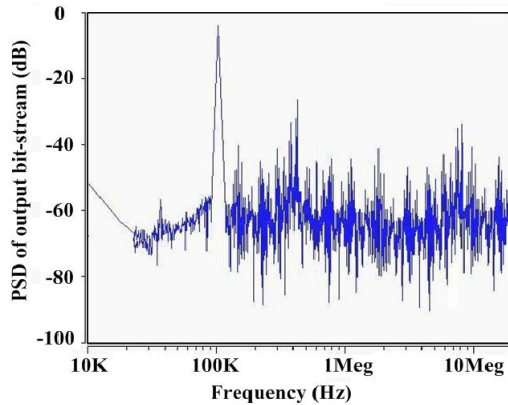


**Figure 7.** Power spectral density in the frequency domain for delay sweep 2 p s (p-p) without first order noise shaping
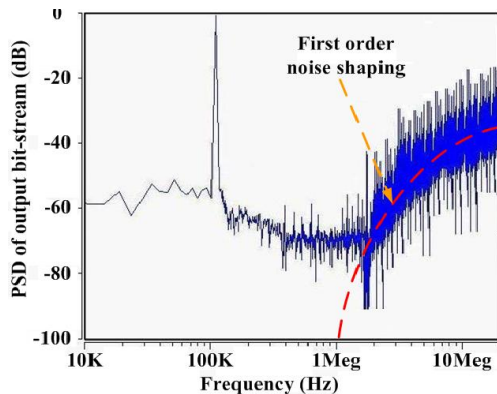


**Figure8.** Power spectral density in the frequency domain for delay sweep 2 p s (p-p) with first order noise shaping

When this VTDC is utilized in the ADFS, shaped high frequency noise can be digitally filtered by digital low pass filter which is implemented in the ADFS.

The linearity performance of the TDC was measured by Differential nonlinearity (DNL) characterization by using a code density test. This test is a one of the common tests which employing in the TDC linearity characterizations.

As shown in Figure 9, the proposed VTDC linearity was tested over periods from 4ps to 8ns interval. Approximately 100000 measurements of each time interval were averaged to reduce statistical variation. The nonlinearity of the VTDC is less than ±4ps (1LSB) for these time intervals inputs. Therefore the DNL test emphasis that a variation in the input time interval of VTDC has a minimal impact on the precision of the VTDC.

Table 1 exhibits a detailed comparison between this work and other TDC realizations. The table illustrates that this TDC has better performance compared to similar devices, especially achieving high resolution below 4ps within 11bit dynamic range.
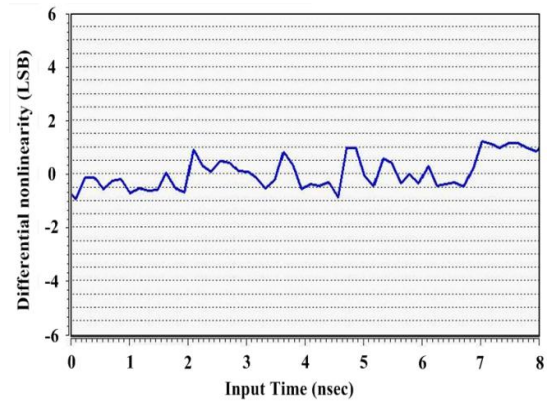


**Figure 9.** Differential nonlinearity performance of VTDC

## 5. Conclusion

In this paper, we have introduced, analyzed, and simulated first order noise-shaping techniques that utilization in the VTDC. In this case, the fundamental ability of this VTDC to perform time interval digitalization with highly digital circuitry was observed to efficiently achieve high-performance ADFS in advanced CMOS technology.

**Table 1. Comparing to previous work**

| Reference | [3] | [6] | [9] | This work |
|---|---|---|---|---|
| Clock Fr. (MHz) | 50 | 15 | 100 | 40 |
| Time Resolution (ps) | 6 | 8 | 97.5 | 4 |
| Noise shaping | Yes | No | No | Yes |
| Dynamic range (bits) | 11 | 11 | 8 | 11 |
| DNL (LSB) | N.A. | N.A. | ±0.3 | < 1 |
| Power (mW) | 21 | 7.5 | 175 | 1.5-16.5 |
| CMOS process (nm) | 130 | 130 | 500 | 180 |

The proposed VTDC has an 11bit dynamic range and 4ps LSB. The linearity test result indicates that the VTDC sustains a DNL under 1LSB.

## References

[1] B. Helal, Techniques for Low Jitter Clock Multiplication, MIT, Ph.D. thesis, 2008, 100-135.

[2] C. Hesu, Techniques for High Performance Digital Frequency Synthesis and Phase Control, MIT, Ph.D. thesis, 2008, 61-87.

[3] M. Straayer, Noise shaping techniques for analog and TDC using voltage controlled oscillator, MIT, Ph.D. thesis, 2008, 124-152.

[4] K. Ok, A Stochastic Time-to-Digital Converter for Digital Phase-Locked Loops, Oregon State University MSC. Thesis, 2005, 25-46.

[5] F. Brandonisio and others, "First Order Noise Shaping Local-Oscillator Based Time-to-Digital Converter," IEEE International Conference on Electronics, Circuits, and Systems, ICECS 2010, 41 - 44.

[6] J. Yu, F. F. Dai and R. Jaeger, "A 12-bit Vernier Ring Time-to-Digital Converter in 130nm Technology ", in IEEE J. of Solid S. Circuits. VOL. 45 NO. 4, 830- 842, Apr. 2010.

[7] B. Helal, M. Straayer, and M. H. Perrott, "A low jitter 1.6 GHz multiplying DLL utilizing a scrambling time-to-digital converter and digital correlation," in VLSI Symp. Dig. Tech. Papers, 166–167, Jun. 2007.

[8] J. Doernberg, H. S. Lee, and D. A. Hodges, "Full-speed testing of A/D converters," IEEE J. Solid-State Circuits, vol. SC-19, 820–827, Dec. 1984.

[9] B. Swann, B. Blalock and others, "A 100-ps Time-Resolution CMOS TDC For Position Emission Tomography, " IEEE J. Solid-State Circuits, vol. 39, NO.11, 1839-1852, Nov.2004.