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New Multiplier/Divider Using a Single Cdba

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Abstract A new multiplier-divider circuit using a single Current Differencing Buffered Amplifier (CDBA) and only six MOSFETs has been presented. The proposed circuit has the advantage of simultaneously realizing a multiplier and divider without changing the circuit topology. The basic functions of the proposed circuit have been verified through PSPICE simulations using a CMOS CDBA and NMOS transistors with process parameters of 0.35 µm CMOS technology and some application results of the proposed cell in various modes of operation have been included.

Keywords: *analog multipliers, Analog Dividers, Current differencing buffered amplifiers, Analog Integrated Circuits, Analog Signal Processing, CMOS Circuits*

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1. Introduction

The Current differencing buffered amplifier (CDBA) [1] and its current-controlled version have received significant attention in literature as they have been shown to offer a lot of flexibility and versatility in analog circuit design, for instance, see [2,3,4,15,16,17,18] and the references cited therein. Several bipolar and CMOS implementations of the CDBA have also been advanced over the years such as those in [1,2,3,4] and [16-22].

The circuit symbol of the CDBA is shown in Figure 1. A CDBA is a four terminal building block which is characterized by the terminal equations

$$V_p = V_n = 0, i_z = i_p - i_n, V_w = V_z \quad (1)$$

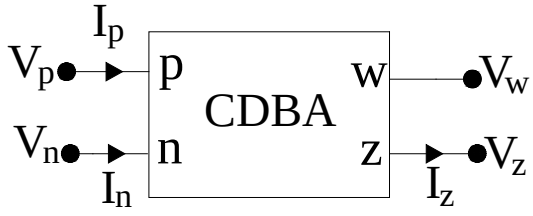

Figure 1. Symbolic notation of the CDBA

Various researchers have proposed analog multiplier and/or divider circuits in the past using a variety of active building blocks such as Current Controlled Current Conveyors (CCCII) [5,7], second generation Current Conveyors (CCII) [6], operational trans-conductance amplifiers (OTA) [8], current differencing trans conductance amplifiers (CDTA) [9], operational amplifiers [10,11,12,19], operational trans-resistance amplifier (OTRA) [13], current feedback operational amplifiers (CFOA) [14], current controllable current conveyor trans conductance amplifier (CC-CCTA) [20], dual-X second-generation current conveyors (DXCCIIs) [21] and current controlled current-differencing trans-conductance amplifiers (CC-CDTA) [22].

These multiplier/divider circuits, however, suffer from one or other problems. For example, the four quadrant multiplier and two quadrant divider reported in [5] has the disadvantage of employing two active elements (CCCII+s) elements are the performance of the circuit is temperature-sensitive. Similarly, the four quadrant analog multiplier presented in [6] also needs two active elements (CCIIs). On the other hand, the current mode (CM) multiplier proposed in [7] based on bipolar CCCII+ uses one active element and a current controlled ground resistor, requires current-matching for successful operation as multiplier, is temperature-sensitive, has non-differential current inputs and suffers from the effects of the parasitic impedances of the CCCII+. The OTA-based CM analog multiplier-divider reported in [8] uses too many active elements (three OTAs). The CM analog multiplier and divider introduced in [9] use two CC-CDTAs but have non-differential inputs. The circuits of [10,11] realize a multiplier/divider using a single op-amp and eight MOSFETs but the circuit employs both positive and negative feedback thereby leading to a condition for the stability while that of [12] although reduces the number of MOSFETs to six but needs two op-amps to realize multiplier/divider. Furthermore, as these circuits [10,11,12] are based on op-amps, their operation is limited by the well-known limitations of the op-amps. Using a single OTRA and eight MOS transistors, an analog multiplier

was reported in [13] but this circuit has the limitation of allowing only non-differential inputs. In [14], Liu reported a circuit using only four MOSFETs and two CFOAs[1], but the circuit therein realizes only a divider. In [19], Riewruja and Rerkratn reported a four-quadrant multiplier using op-amps but the circuit requires as many as five op-amps and eleven resistors and is hence, not economical. Woratraijariya, Mano, Jaikla, and Maneewan in [20] reported a CM four quadrant divider, using a single CC-CCTA but the circuit can perform only the operation of a divider. Kumngern [21] presented a four-quadrant multiplier based on two DXCCIIs but the circuit can perform only multiplication. Siripruchyanun and Jaikla [22] introduced a CM analog multiplier/divider based on CC-CDTA but circuit can operate as multiplier/divider for only two quadrants.

On the other hand, among the multipliers/dividers employing CDBAs known earlier, the circuit of [15] employs a single CDBA along with only four MOSFETs but realizes only a multiplier. Siripruchyanun [16] presented a CM analog multiplier and divider using two CC-CDBA [17] but their circuit provides only two quadrant operation as a multiplier. Jaikla and Siripruchyanun in [18] also reported a CM analog multiplier and a divider but their circuits require three and two CC-CDBAs respectively. Another significant drawback of the circuits of [17,18] is that different circuit topologies are required for multiplier and divider operations.

In contrast to the above mentioned circuits, this paper proposes a new CDBA-based circuit which uses only a single CDBA along with only six MOSFETs but offers the significant advantages of (i) simultaneous realisability of a multiplier as well as a divider from the same configuration and (ii) independence of the output of the configuration from the aspect ratios of the MOSFETs if all of them are assumed to be matched (on the other hand, different aspect ratios of input and output MOS transistors can be used to have a desired gain factor). The workability of the proposed circuit, in its various application modes, has been verified by SPICE simulations employing the CMOS CDBA architecture of [2] using 0.35 µm CMOS technology and some sample application results have been presented.

2. The Proposed Multiplier/Divider Cell

Figure 2 shows the proposed multiplier/divider cell. Considering n-channel MOS transistors operating in triode region and assuming the aspect ratios of M_1 to M_4 as (W_i/L_i) and that of M_5 and M_6 as (W_o/L_o), and using the characterizing equation (1) of the CDBA, the interrelationship between the drain currents of the various MOSFETs can be written as

$$I_{d_1} + I_{d_2} + I_{d_5} - I_{d_3} - I_{d_4} = I_{d_6} \tag{2}$$

Using drain current equation of all the MOSFETs operating in triode region in terms of V_{gs} and V_{ds}, from (2), the voltage output of the circuit is found to be

$$V_o = \frac{\left(W_i/L_i\right)}{\left(W_o/L_o\right)} \frac{\Delta X \Delta Y}{\Delta Z} \tag{3}$$

where $\Delta X = (X_1 - X_2)$, $\Delta Y = (Y_1 - Y_2)$ and $\Delta Z = (Z_1 - Z_2)$. Thus, like the circuits of [5,6], the proposed circuit can perform the computation of $(\Delta X \Delta Y/\Delta Z)$ where all the signals are differential input voltages and if aspect ratios of all MOS transistors are taken to be same, the output voltage becomes independent of the parameters of the MOS transistors.

In order to keep operation of all the MOS transistors in the linear region one requires:

For M_1 to M_4

$$Y_1, Y_2 \le \min[(X_1 - V_T), (X_2 - V_T)] \tag{4}$$

For M_5 to M_6:

$$V_o \le \min[(Z_1 - V_T), (Z_2 - V)_T] \tag{5}$$

where V_T is the threshold voltage of the MOS transistors.

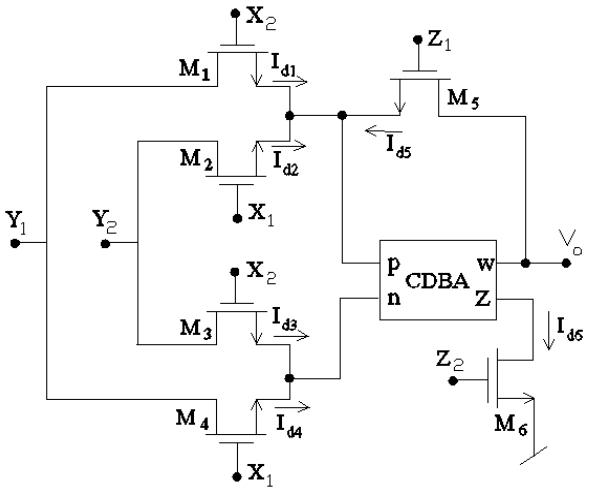

Figure 2. The proposed Multiplier/Divider cell

3. SPICE Simulation Results

To verify the workability of the proposed configuration, a number of its applications have been checked through SPICE simulations using the CMOS CDBA of [2] biased with ±5V DC supply while using MOS transistors with 0.35 μm CMOS process parameters.

3.1. Analog Divider

For checking the divider operation, input signals were applied at Y and Z terminals and the control voltages were applied at X terminal of the MOSFETs. Taking $Y_1 = Y_2 = y$, $X_1 = Vc_1$ and $X_2 = Vc_2$, $Z_1 = (Z + z)$ and $Z_2 = (Z - z)$, where Z is the DC bias at gate terminal of M_5 to M_6 and Vc_1, Vc_2 are DC control voltages, we obtain output voltage as

$$V_o = (V_{c2} - V_{c1}) \frac{\left(W_i/L_i\right)}{\left(W_o/L_o\right)} \frac{y}{z} \tag{6}$$

[1] A closer look at the circuit of Fig.3 of [14] reveals that the composite connection of the two CFOAs therein is exactly configured as a CDBA! Hence, the two-CFOA-based analog divider of Fig.3 of [14] can also be considered to be single-CDBA-four-MOSFETs-based analog divider.

The conditions required to keep operation of the MOS transistors in the linear region are given by

For M_1 to M_4:

$$y \le \min[(V_{c1} - V_T), (V_{c2} - V_T)] \quad (7)$$

For M_5 to M_6:

$$z + V_o \le (Z - V_T) \quad (8)$$

In SPICE simulations of the divider circuit, V_{c1} and V_{c2} were kept at 5.0V and 4.95V respectively while Z was kept at 4.5V. The input signal z was varied from -2V to -0.6V and y signal was varied from -0.2V to 0.2V in steps of 0.1V. With all MOSFETs having same aspect ratios, the simulation results and theoretical results are shown in Figure 3 which are found to be closely matching with the theoretical ones.

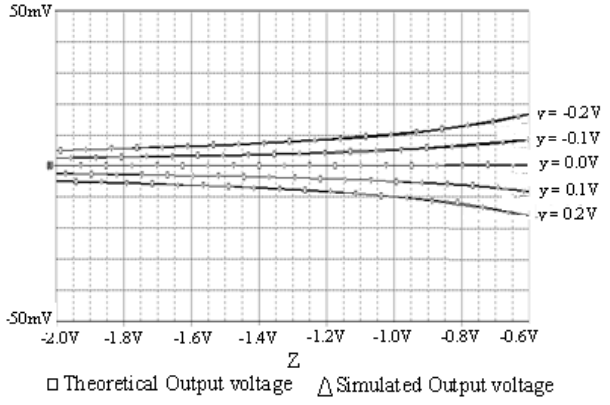

Figure 3. DC transfer characteristics of the proposed configuration used as a divider

3.2. Analog Multiplier

In this case, the input signals are applied at the X and Y terminals. Let $Y_1 = -Y_2 = -y$, $X_1 = (X+x)$ and $X_2 = (X-x)$, $Z_1 = Vc_1$ and $Z_2 = Vc_2$, where X is the DC bias at gate terminal of M_1 to M_4 and Vc_1, Vc2 are DC control voltages. Using these signals and control voltage, we obtain the output voltage of the circuit as

$$V_o = \frac{4\left(W_i / L_i\right)}{\left(W_o / L_o\right)} \frac{xy}{(V_{c2} - V_{c1})} \quad (9)$$

The condition required to keep operation of the MOS transistors in the linear region is given by

For M_1 to M_4:

$$(x + y) \le (X - V_T) \quad (10)$$

The widths and lengths of M_1 to M_6 were taken as 2.8 µm and 0.35 µm respectively; X was kept at 4.0V while V_{z1} and V_{z2} were kept at 3.75V and 5V respectively. The x input signal was varied from –0.23V to 0.23V and y signal was varied from -180mV to 180mV in step of 90mV. Figure 4 shows the simulation results which are seen to be in good agreement with the theoretical ones.

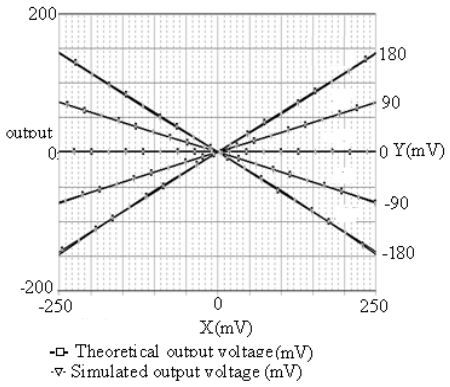

Figure 4. DC transfer characteristics of the proposed configuration as a multiplier

3.3. Squarer

For using the circuit as a squarer, X was kept at 4.5V while V_{z1} and V_{z2} were kept at 3.75V and 5V respectively. The inputs x and y were both taken as sinusoidal signals of 1 KHz, zero avg., 200mVpp. Figure 5 shows the simulation results of the proposed configuration as a squarer.

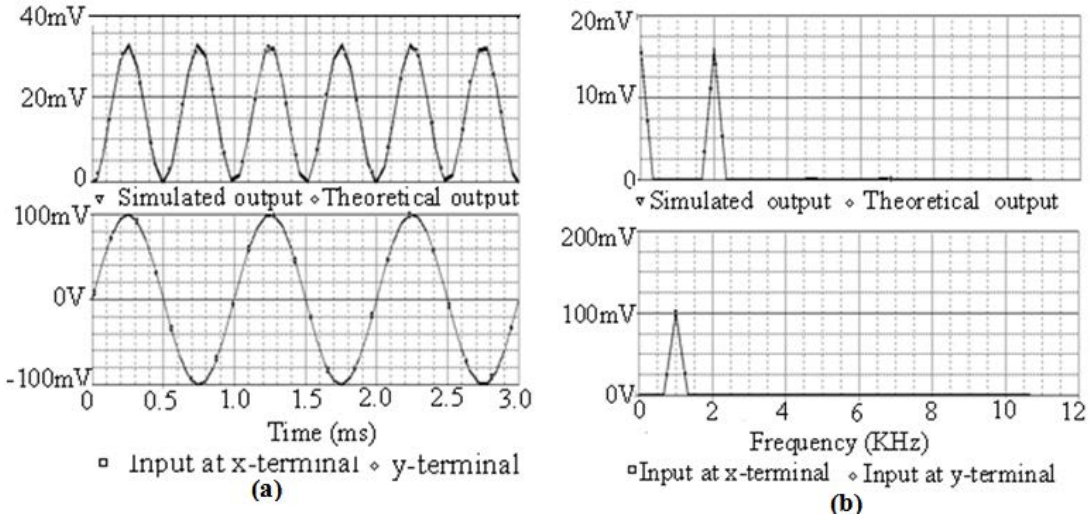

Figure 5. Simulation results of the proposed cell as a squarer (a) time response (b) frequency spectrum

3.4. Modulator

To verify the operation of the proposed configuration as a modulator, X was kept at 4.5V while V_{z1} and V_{z2} were kept at 3.75V and 5V respectively. The input x was

sinusoidal signal of 1 KHz, zero avg., 200mVpp while y was taken as a sinusoidal signal of 10 KHz, zero avg., 200mVpp. Figure 6 shows the simulation results of the circuit as a modulator.

The SPICE simulation results of Figure 3-Figure 6, thus, establish the workability of the proposed configuration in its various modes of operation.

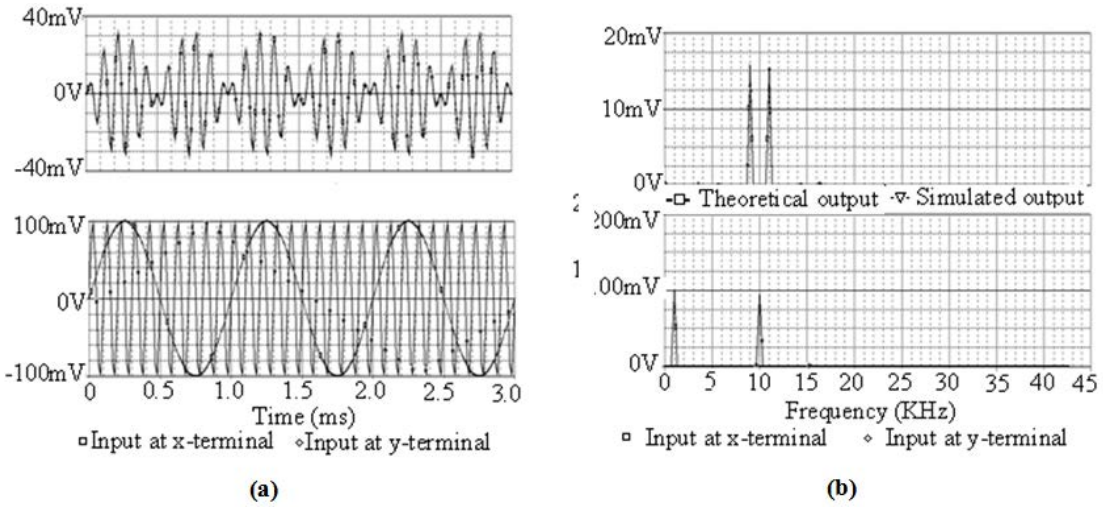

Figure 6. Simulation results of the proposed configuration as a squarer (a) time response (b) frequency spectrum

3.5. Frequency Characteristics of the Proposed Configuration

In this case, the input X was kept at 4V while V_{z1} and V_{z2} were kept at 3.75V and 5V respectively. The input x was taken as a sinusoidal signal of amplitude 1mV of varying frequency and y was taken as a DC signal of 0.1V. Figure 7 shows the frequency response of the proposed configuration obtained through SPICE simulations which is seen to exhibit a bandwidth of around 82.3MHz.

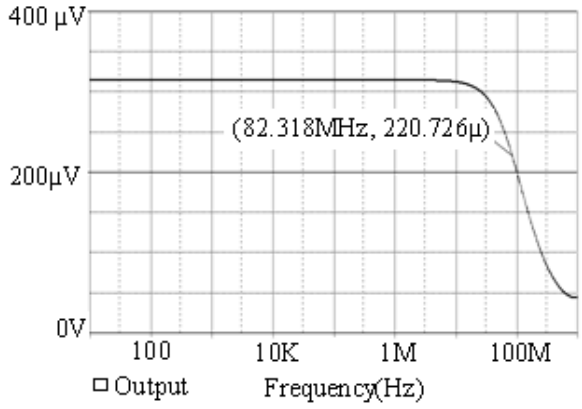

Figure 7. Frequency response of the proposed Multiplier/Divider cell obtained through SPICE simulations

4. Concluding Remarks

A new multiplier/divider cell based on a single CDBA is presented. While previously known single-CDBA-four-MOSFETs-based circuits can realize only a multiplier as in [15] or only a divider as in [14] (with the two CFOAs employed therein configured *exactly equivalent* to a CDBA as mentioned in footnote 1), the presented single-CDBA-based configuration uses six MOSFETs but has the advantage of realizing both multiplier and divider functions simultaneously. SPICE simulation results based on CMOS CDBA and MOS transistors in 0.35um CMOS technology have confirmed the workability of the proposed configuration in its various modes of operation. The layout of the proposed cell using CMOS CDBA architecture from [2] has shown the chip area of the circuit as 0.015mm^2 (layout area without pads).

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