

New Squaring and Square-rooting Circuits Using Cdba

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Abstract One new squaring and two new square-rooting circuits based on CDBAs have been introduced. The new squarer circuit consists of a CDBA, two NMOS transistors and one resistor. On the other hand, the first square-rooting circuit consists of two CDBAs, two NMOS transistors while the second square-rooting circuit consists of only a single CDBA, two NMOS transistors and two PMOS transistors. The proposed circuits exhibit wide input voltage range, very small error and offer low output impedance to facilitate easy cascading without requiring additional buffers. PSPICE simulation results are included which confirm the practical workability of the new circuits.

Keywords: squarer, square-rooter, current differencing buffered amplifier

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1. Introduction

Squaring and square-rooting circuits are widely used for continuous-time signal processing in measurement and instrumentation systems [1]. In order to maintain compatibility with existing voltage processing circuits as well as taking advantages [2] of the current-mode circuits, the new active element called Current differencing buffered amplifier (CDBA) [3] has received significant attention in literature since it can operate in both current-mode as well as voltage-mode. In earlier literature, the CDBA has been shown to offer a lot of flexibility in linear analog circuit design [3,4,5,6]. However, the use of CDBA in realizing non-linear functions has rather been limited [7,8,9].

The purpose of this paper is to present new squaring and square-rooting circuits based on CDBAs. The proportionality constant of the new circuits can be controlled by the value of an external resistor. The effectiveness of the proposed circuits is verified through SPICE simulations.

2. The Current-differencing Buffered Amplifier (CDBA)

A practical CDBA can be described by the following relationships that take into account the various non-idealities:

$$V_p = V_n = 0, I_z = \beta_p I_p - \beta_n I_n, V_w = \alpha V_z \quad (1)$$

where $\beta_p = 1 - \varepsilon_p$ and ε_p ($|\varepsilon_p| \ll 1$) is the current tracking error from p-terminal to z-terminal, $\beta_n = 1 - \varepsilon_n$ and ε_n ($|\varepsilon_n| \ll 1$) is

the current tracking error from n-terminal to z-terminal, and $\alpha = 1 - \varepsilon_v$ and ε_v ($|\varepsilon_v| \ll 1$) is the voltage-tracking error from z-terminal to w-terminal of the CDBA. The circuit symbol of the CDBA is shown in Figure 1.

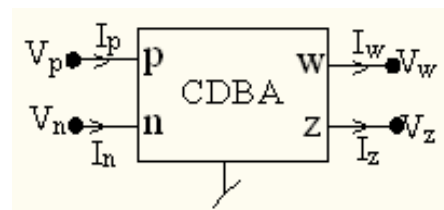


Figure 1. Symbolic notation of the CDBA

3. Squarer Circuit

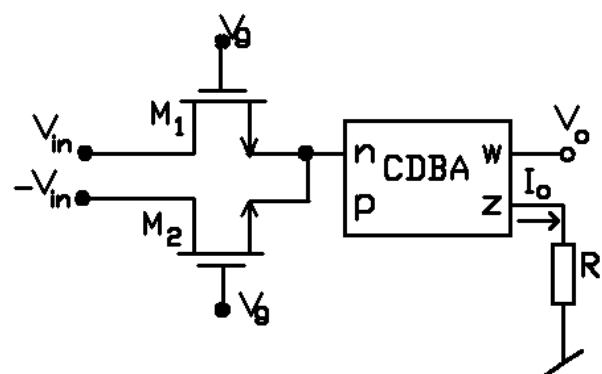


Figure 2. The proposed squarer circuit

Figure 2 shows the proposed squarer circuit. Assuming matched MOS transistors operating in triode region, a straight forward analysis of the circuit gives

$$V_o = \frac{\alpha\beta_n KWRV_{in}^2}{L} = \frac{V_{in}^2}{V_{ref}} \quad (2)$$

where V_{ref} is the proportionality constant, (W/L) is the aspect ratio of MOS transistors, $K=\mu_n C_{ox}$ is the process trans-conductance parameter of the MOS transistor. The proportionality constant V_{ref} can be controlled by resistor R .

The output current I_o is given by

$$I_o = \frac{V_o}{R} = \frac{\beta_n KRV_{in}^2}{L} = dV_{in}^2 \quad (3)$$

where d is the proportionality constant. Thus, the circuit can work in trans-admittance mode also.

4. Square-rooting Circuits

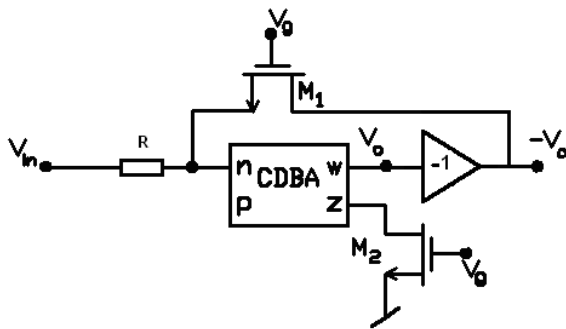


Figure 3. The first proposed square-rooting circuit

Figure 3 shows the first proposed square-rooting circuit. Assuming MOS transistors M_1 and M_2 to be matched and operating in triode region, the output voltage is found to be

$$V_o = \sqrt{\frac{2L_1 V_{in}}{KW_1 R \beta_n (1 + \beta_n \alpha^2)}} = b\sqrt{V_{in}} \quad \text{for } V_{in} > 0 \quad (4)$$

where b is the proportionality constant, (W/L) is the aspect ratio of MOS transistors, $K=\mu_n C_{ox}$ is the process trans-conductance of the MOS transistor and the proportionality constant b can be controlled by the resistor R . It is interesting to point out that the same circuit can work for the negative value of V_{in} if we connect R to p-terminal instead of n-terminal of the CDBA.

In the derivation of equation (4), to enable the cancellation of the non-linear terms, $L_1=L_2$ and $W_2=\alpha^2\beta_n^2W_1$ have been taken where (W_1/L_1) and (W_2/L_2) are the aspect ratios of the MOS transistors M_1 and M_2 respectively.

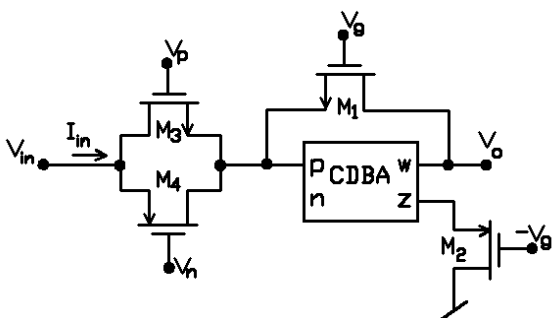


Figure 4. The second proposed square rooting circuit

Figure 4 shows the second proposed square-rooting in which the MOS transistors M_1 and M_2 are operating in triode region and are used to obtain the basic square-rooting function. The MOS transistors M_3 and M_4 are also operating in the triode region and are used to realize floating voltage controlled resistor [10]. After taking the model parameters of the CMOS process from [11], $V_g=2.63V$, $L_1=L_2$, $W_1=0.2455W_2$, a routine analysis of the proposed circuit then gives the following expression for its output voltage

$$V_o = \sqrt{\frac{2\alpha^2\beta_p L_1 V_{in}}{R_{eq}(K_p W_2 + K_n W_1 \beta_p \alpha^2)}} = e\sqrt{V_{in}} \quad \text{for } V_{in} > 0 \quad (5)$$

where e is the proportionality constant, (W_1/L_1) and (W_2/L_2) are the aspect ratios of MOS transistors M_1 and M_2 respectively, $K_n=\mu_n C_{ox}$ and $K_p=\mu_p C_{ox}$ being the process transconductances of the NMOS and PMOS transistor respectively.

Here, the proportionality constant e can be controlled by the resistor R_{eq} which is given by

$$R_{eq} = \frac{V_{in}}{I_{in}} = \frac{L_3}{KW_3(V_n - V_p - V_{tn} + V_{tp})} \quad (6)$$

where (W_3/L_3) is the aspect ratio of the MOS transistor M_3 , V_n and V_p are the gate voltages of M_3 and M_4 respectively, V_{tn} and V_{tp} are the threshold voltage of M_3 and M_4 respectively. To cancel non-linear terms, W_4 is taken equal to $\mu_n W_3 / \mu_p$.

The same circuit can work for the negative value of V_{in} if we connect the CMOS transistors constituting R_{eq} to the n-terminal of the CDBA instead of the p-terminal.

5. SPICE Simulation Results

To verify the theoretical results, the squarer circuit has been simulated in SPICE using the CDBA from [11] operating at $\pm 5V$ DC supply with $0.35 \mu m$ CMOS process parameters. The value of R is made equivalent to $\frac{L}{10\alpha\beta_n KW}$ so that proportionality constant becomes equal to 10.

Using SPICE, the values of α , β_p and β_n of the CDBA were found to be 1.0000998, 1.002501 and 1.002501 respectively. With $L_1=L_2=28 \mu m$, $W_1=W_2=35 \mu m$, the value of R , to make proportionality constant equal to 10, has been adjusted to 990Ω . Figure 5 shows the DC transfer characteristics of the proposed squarer circuit. Figure 6 shows the transient response of the circuit to a sinusoidal input of $4V_{pp}$, having zero average value and frequency of 1 kHz.

The square rooting circuit 1 of Figure 3 has been simulated in SPICE using the CDBA [11] operating at ± 5 Volts DC supply with $0.35 \mu m$ CMOS process parameters. In the simulations the value of R is made equivalent to $\frac{2L_1}{W_1\beta_n K(1 + \beta_n \alpha^2)}$ so that the proportionality constant b becomes equal to 1. To realize unity gain inverting amplifier, a CDBA-based inverter has been used. By

selecting $L_1=L_2=21 \mu\text{m}$, $W_1=21 \mu\text{m}$ then $W_2=\alpha^2\beta_n^2W_1$ comes out to be approximately equal to $21 \mu\text{m}$. To get unity proportionality constant b , the value of R was adjusted to $12 \text{ k}\Omega$. Figure 7 shows the DC transfer

characteristics of the proposed square-rooting circuit. Figure 8 shows the transient response of the circuit to a sinusoidal input of $1V_{pp}$, average of 0 Volts and frequency of 1 kHz .

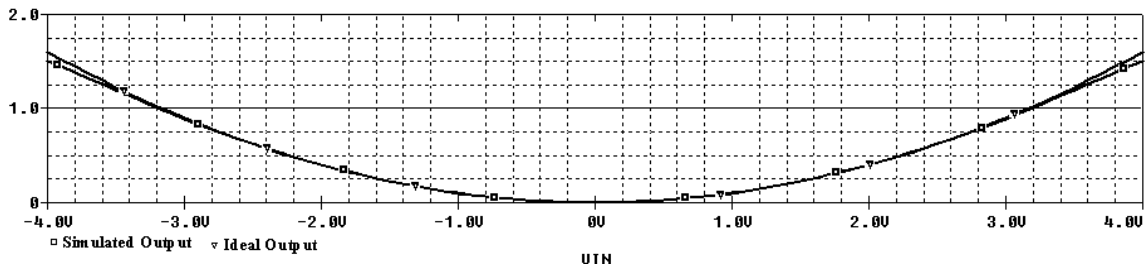


Figure 5. DC transfer characteristics of the proposed Squarer Circuit for $R=990\Omega$

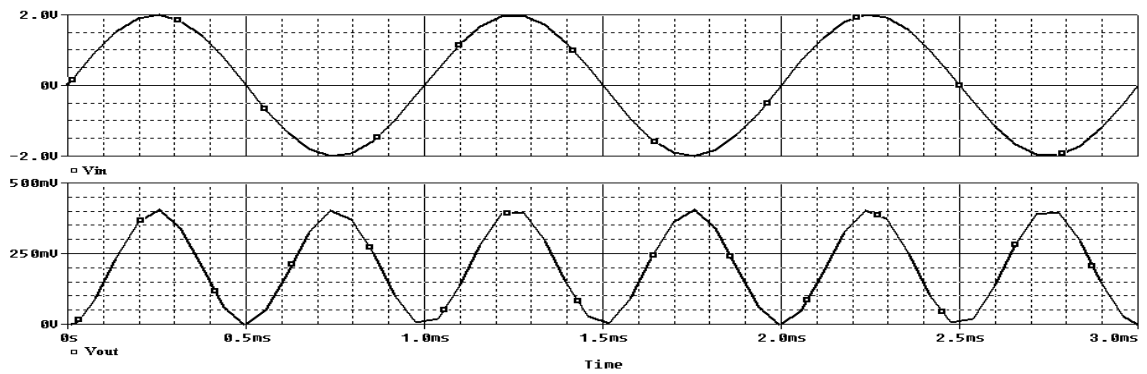


Figure 6. Output voltage waveform obtained from the proposed Squarer circuit for 1 KHz Sinusoidal input

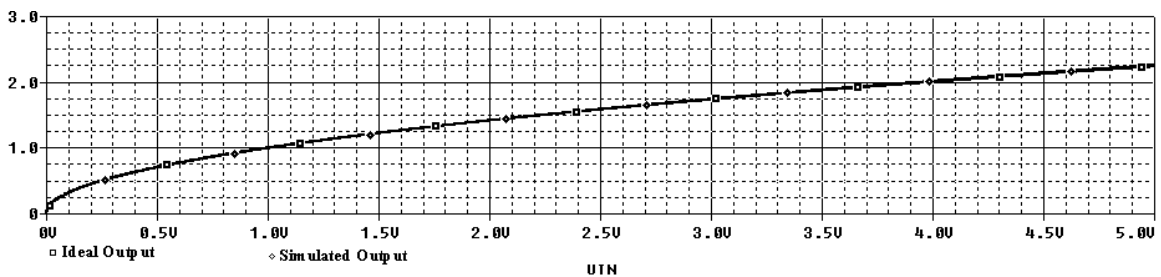


Figure 7. DC transfer characteristics of the Square rooting circuit 1

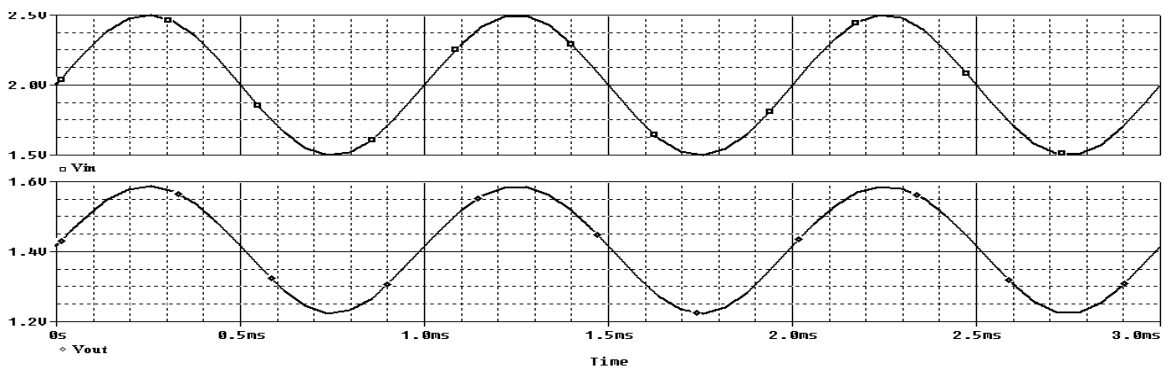


Figure 8. Output voltage waveform obtained from the Square rooting circuit 1 for 1 KHz Sinusoidal input

In the simulations of the square rooting circuit 2 of Figure 4, CDBA from [3] was used operating at $\pm 12V$ DC supply with the value of R_{eq} made equivalent to

$$\sqrt{\frac{2\alpha^2\beta_pL_1}{(K_pW_2 + K_nW_1\beta_p\alpha^2)}}$$
 so that proportionality constant e becomes equal to 1. By selecting $L_1=L_2=24 \mu\text{m}$,

$W_2=40 \mu\text{m}$ then $W_1=0.2455W_2$ comes out to be equal to $81.45 \mu\text{m}$. To obtain unity proportionality constant, the value of R_{eq} was adjusted to 8722Ω by selecting $L_3=L_4=67 \mu\text{m}$, $W_3=15 \mu\text{m}$, $W_4=57.11 \mu\text{m}$, $V_p = 4V$ and $V_n = -4V$. The circuit of Figure 4 was also simulated using the same aspect ratios of MOS transistors and adjusted value of R_{eq} . Figure 9 shows the DC transfer characteristics of the square rooting circuit. Figure 10

shows the transient response of the circuit to a sinusoidal input of $1V_{pp}$, average of 0.5V and frequency of 1 kHz. Apart from the DC transfer characteristics and transient

response of the proposed circuits, Table 1 shows the input voltage range, % error for this range and the band width of the proposed circuits.

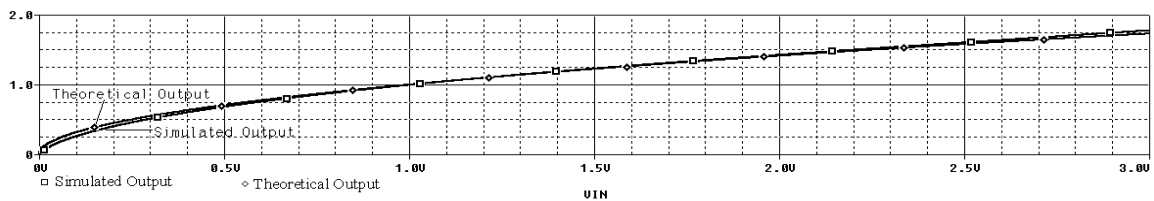


Figure 9. DC transfer characteristics of the square rooting circuit 2

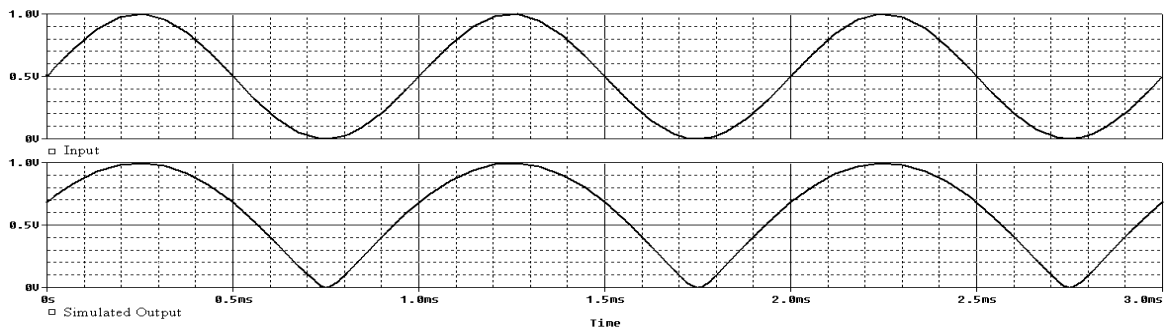


Figure 10. Output voltage waveform obtained from the square rooting circuit 2 for 1 KHz sinusoidal input

Table 1. Input voltage range, % error and band width of the proposed circuits

Parameters	Squarer circuit	Square rooting circuit 1	Square rooting circuit 2
Input voltage range (v)	-3.53 to 3.53	0 to 5.0	0.6 to 3.0
$\% Error = \left \frac{I_{output} - S_{output}}{I_{output}} \right \times 100\%$	Less than 2.5%	Less than 1.0%	Less than 2.0%
Band width (MHz)	30.0	3.46	2.04
where I_{output} = Ideal value of output, S_{output} = Simulated value of output			

6. Comparison with the Existing CDBA-Based Squarer and Square Rooting Circuits

Squarer circuit can also be realized from the four quadrant multiplier proposed by Keskin in [7] by taking two input signals to be same but such a realization will need an additional summer and difference circuits also. By contrast, in the proposed squarer circuit, only an additional inversion circuit is required. On the other hand, the current-mode squarer proposed by Lawanwisut and Siripruchyanun [9] needs four current-controlled CDBAs against one as required by the proposed squarer circuit. Furthermore, no square-rooting circuit has been reported earlier using CDBAs.

As compared to the squarer circuit based on Current Conveyors (CC) [12], the proposed squarer circuit has low output impedance to facilitate easy cascading without the need of additional buffers. Also, the band width of the proposed square-rooting circuits is 3.46 MHz as compared to 400 kHz for the CC-based square-rooting circuit of [12]. Furthermore, the proposed square-rooting circuit 1 employs only two active elements and the square-rooting circuit 2 employs only one active element as compared to three active elements (one CCII+ and two op-amps) used in the CC-based circuits of [12].

7. Concluding Remarks

New squarer and square-rooting circuits based on the CDBA have been proposed. These circuits exhibit wide input voltage range, smaller errors and have a low output impedance to facilitate easy cascading without requiring additional buffers. The proportionality constant of these circuits can be controlled by the value of an external resistor. Squarer circuit also works in trans-admittance mode. SPICE simulations have verified the workability of the proposed circuits.

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