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CMOS Voltage-Controlled Negative Resistance Realization

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Abstract In this communication, a new CMOS circuit configuration is proposed to realize a voltage-controlled negative resistance (VCNR) which has been implemented using only eight MOS transistors- all working in the saturation region. The value of the realized negative resistance is controlled by two identical and opposite external DC voltages. The workability of the proposed circuit has been confirmed by Cadence Virtuoso simulations and some sample results have been given. The proposed VCNR circuit has been shown to exhibit good linearity, has good variable negative resistance range from -1.05kΩ and -300Ω and offers a good operational frequency range up to around 100 MHz with total power dissipation between 0.5mW- 8.73mW only.

Keywords: *JFET, MOSFET, CMOS, voltage-controlled resistance, voltage-controlled negative resistance*

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1. Introduction

In recent years, electronically-controllable resistors are preferred for integrated circuit (IC) applications and implementations rather than passive resistors fabricated on the IC chips because the latter occupy relatively much larger chip area and have limited accuracy. On the other hand, actively-simulated resistors are extremely suitable because they require considerably reduced chip area and provide electronic-controllability of their values through an external voltage or current. Thus, the voltage-controlled resistances (VCR) are attractive components for many electronically-controllable functional circuits such as voltage-controlled filters, voltage-controlled oscillators (VCO), voltage-controlled phase-shifters, and several others.

Motivated by the above, there have been many studies on the realization of electronically-controllable resistors in the earlier literature, for instance, see [1-31]. In earlier works, there are some VCR circuits which were devised based upon the use of JFETs [1-7,17,18,26,28,30] while some current-controlled resistances using BJTs have also been proposed such as those in [8,9]. On the other hand, the grounded VCRs proposed in [10-16,21-24] employ MOS transistors operating in triode/saturation regions in which those operating in the former regime exhibit a square nonlinearity in the expression of their drain current which is canceled with an appropriately devised additional MOS-transistors-based circuitry. Many such *linearized* VCRs or more general *linearized* voltage-controlled impedances based upon such ideas of *nonlinearity-cancellation* have also been formulated with the help of a variety of analog building blocks such as operational amplifiers [2-5,7,17,18], Operational transconductance amplifiers (OTA) [19], second-generation Current Conveyors (CCII) as in [6] (also see [7] and [26]), current feedback op-amps (CFOA) along with a JFET/MOSFET and a few resistors, as in [28,30] and CFOAs and an analog multiplier as in [29]. Lastly, it must also be pointed out that a low power VCR has also been devised using an FGMOS transistor in [20].

From the survey of the earlier published literature, it has been revealed that while a large number of circuits//techniques have been advanced for realizing voltage-controlled positive resistances (VCPR), comparatively fewer circuits have been evolved to realize voltage-controlled negative resistances (VCNR). The various previously known VCNR circuits are as follows:

In reference [8], a two-op-amp-FET-based VCNR is presented while references [17], [18] have presented *universal* voltage controlled impedance (VCZ) configurations employing two and three op-amps respectively, besides a JFET and a few resistors, both of which can be configured either as VCPR or VCNR as special cases. However, these propositions suffer from the drawback of requiring a larger number of total active and passive components. On the other hand, the floating VCNR presented in [25] is based upon CMOS technology using the method of conversion of transconductance to resistance but this circuit employs two op-amps also. Lastly, [27] deals with a floating VCNR as a special case, realizable with two operational mirrored amplifiers (OMA), a JFET and a number of passive resistors. The general configurations of [28,30] can realize *grounded* VCNRs using two CFOAs and *floating* VCNRs using three or more CFOAs along with a single JFET/MOSFET and a few resistors. On the other hand, the three-CFOA-one analog multiplier-based circuits of [29] suffer from the use of an excessive number of active elements besides requiring a few passive resistors as well. In reference [31] a second generation current conveyor (CCII+) is used as a negative impedance convertor (NIC) to design a VCNR.

Recently, Yuce, Minaei, and Alpaslan in [10] presented a grounded VCPR circuit which employs only eight MOSFETs and is, thus, very economical and suitable for implementation in CMOS technology. In fact, this circuit, employing only eight MOSFETs can be considered to be the simplest and most economical circuit for realizing a grounded VCPR evolved so far. However, to the best of the present authors' knowledge, any equally simple and economical circuit for realizing a VCNR was neither hinted or implied in [10] nor has subsequently been presented in the literature by the same or any other author so far.

The main intention of this communication is, therefore, to present a VCNR configuration which has been derived by an appropriate rearrangement of the basic MOS sub-circuits employed in the grounded VCPR of [10] and therefore, employs only eight MOSFETs like the circuit of [10].

The workability and the performance of the presented VCNR configuration have been demonstrated by the results of the simulations on CADENCE Virtuoso using 180 nm CMOS technology parameters.

2. The Proposed VCNR Configuration

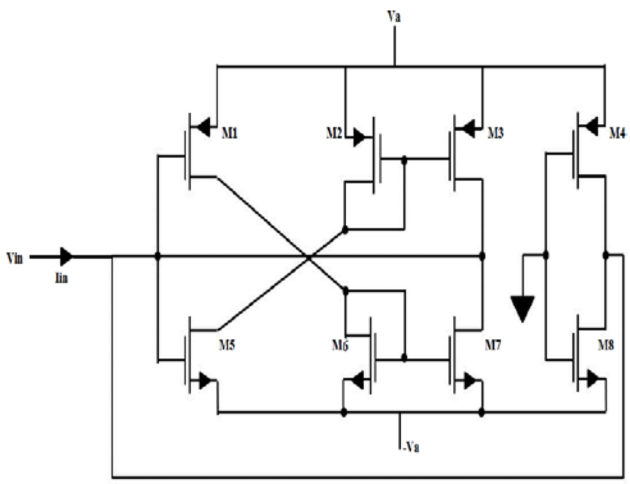

Figure 1. The proposed NVCR configuration

The proposed CMOS circuit is shown in Figure 1 which contains eight MOS transistors all operating in saturation region. The following condition must be followed by the input voltage and DC bias voltages of this VCNR for ensuring the operation of all the MOSFTs in saturation:

$$-V_A + V_{TN} < V_{in} < V_A - |V_{TP}|. \tag{1}$$

Ignoring the channel length modulation effect, the equations for the drain currents of the various MOS transistors can be written as follows:

$$I_{d1} = \frac{k_{p1}}{2}(V_A - |V_{TP}| - V_{in})^2 \tag{2}$$

$$I_{d4} = \frac{k_{p4}}{2}(V_A - |V_{TP}|)^2 \tag{3}$$

$$I_{d5} = \frac{kn_5}{2}(V_{in} + V_A - V_{TN})^2 \tag{4}$$

$$I_{d8} = \frac{k_{n8}}{2}(V_A - V_{TN})^2 \tag{5}$$

where V_{TN} and V_{TP} are the threshold voltages of NMOS and PMOS transistors respectively. All PMOS transistors M_i, i=1-4, all NMOS transistors M_j, j=5-8 are assumed to be identical, however, the transconductance parameters are assumed to be $k_{pi} = \mu_p C_{ox} \frac{W}{L}$ and $k_{nj} = \mu_n C_{ox} \frac{W}{L}$. Mobility is denoted by the symbol μ_n (for NMOS) and μ_p (for PMOS), C_{ox} is the oxide capacitance of both the type of MOS transistors and W/L is the aspect ratio of all the MOS transistors which is assumed to be the same.

In the circuit, the two current mirrors (M_2 - M_3 , and $M_6 - M_7$) are used to copy the drain currents of M_5 and M_1 respectively by assuming that the MOS transistors of both the current mirrors are matched.

The input node equation can now be written as:

$$I_{in} = I_{d1} - I_{d4} - I_{d5} + I_{d8}. \tag{6}$$

By solving equations (2)-(6), the input resistance of the circuit, with k_p= k_n= k for all MOSFETs, is found to be:

$$Req = \frac{V_{in}}{I_{in}} = -\frac{1}{k\left(2V_A - V_{TN} - |V_{TP}|\right)}. \tag{7}$$

Thus, the circuit realizes a VCNR whose value is controllable through V_A, subject to the satisfaction of the conditions dictated by (1).

It may be noted that the DC voltages V_A and $-V_A$ are both DC bias supply voltages and as well as the controlling voltages which may be used to vary the value of the negative resistance realized. Thus, it may be noted that, in contrast to the circuit of [10] which employs two dual DC power supplies, we use only a single dual supply.

3. Simulation Results

The simulation of the VCNR of Figure 1 was carried out on CADENCE at gpdk 180nm technology. The sizing of the MOS transistors was done such that every PMOS had W/L ratio of 23.75µm/1µm and W/L ratio of all the NMOS was 7.5µm/1µm. Figure 2 shows the I-V characteristic for different values of the control voltage (V_A). Applying a DC current I_{in} at the input and sweeping the same, the DC analysis was performed. The good linearity of the realized negative resistance and its variability with control voltage is established from the plots of Figure 2.

Figure 3 shows the variation of Req with the controlling voltage V_A. The value of negative resistance has been found to vary between -1.05kΩ to -300Ω.

To determine the operational frequency range of the proposed VCNR circuit, the magnitude of

Req at different frequencies was determined which is shown in Figure 4. The bandwidth of the circuit when realizing different values of Req at different values of the control voltages ($V_A = 0.75V$, $0.9V$, $1.05V$, $1.2V$, $1.35V$, $1.5V$) are found to be around 100 MHz.

The graph of power dissipation with applied control voltage is shown in Figure 5. The maximum power dissipation was found to be 8.73mW while the minimum was of the order of 0.5mW.

The overall performance of the proposed VCNR was, thus, found to be quite satisfactory.

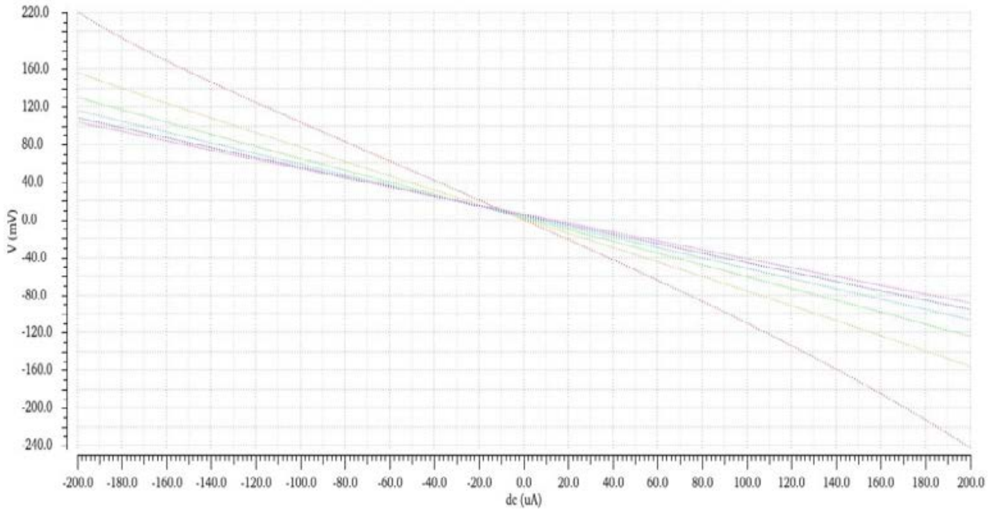

Figure 2. I-V characteristics of VCNR at different V_A (=0.75, 0.9, 1.05, 1.2, 1.35, 1.5) Volts

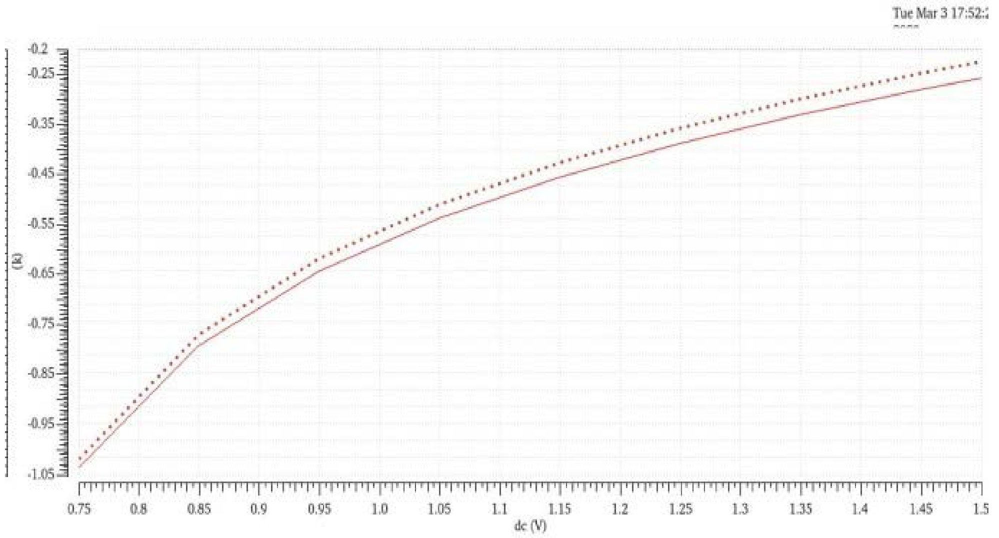

Figure 3. Req versus control voltage

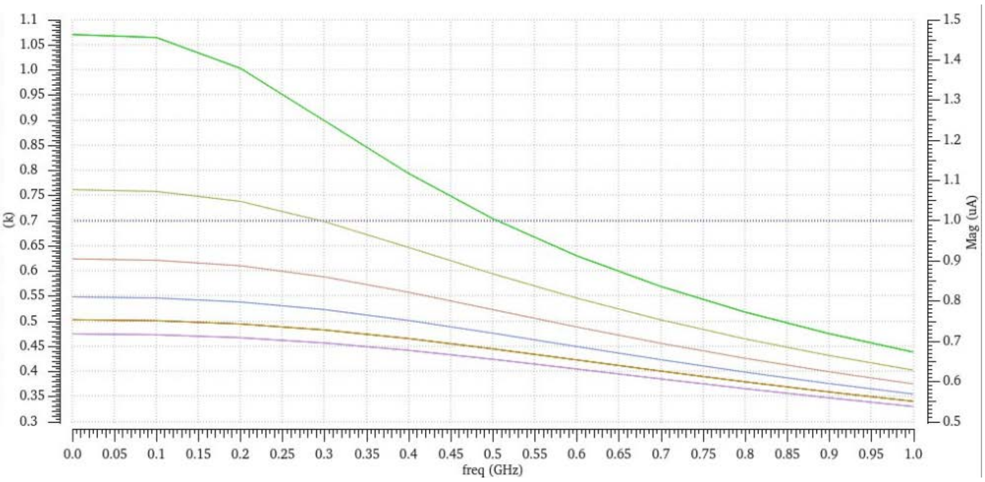

Figure 4. Magnitude |Req| versus frequency at different V_A

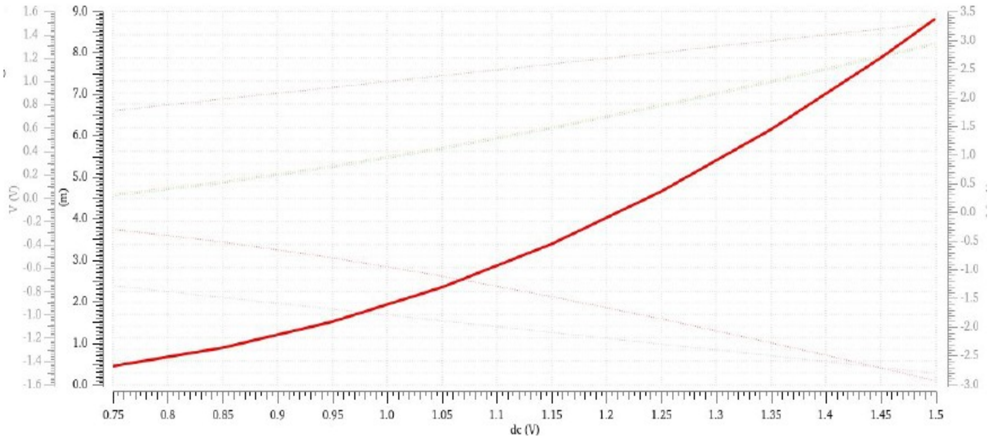

Figure 5. Total power dissipation of the proposed VCNR circuit

Table 1. Comparative Analysis of Earlier VCNRs Available in Literature Designed Without any Active Building Blocks

Parameters	[8]	[20]	[25]	Proposed CMOS VCNR
Type and number of active elements used	28 BJTs	6 FGMOS transistors	1 JFET, a VCCS, several passive resistors and 32 BJTs	8 MOSFETs
Technology Used	Bipolar	FGMOS, 500nm	JFET, Bipolar	CMOS, 180nm GPDK
Linear Range of Operation	I_{in} = ±80μA, V_r = ±40mV	I_{In} = ±30μA, V_r = ±200mV	I_{In} = ±8mA, V_r = ±3V	I_{In} = ±200μA, V_r = ±220mV
Operating Frequency Range	--	420MHz	1MHz	100MHz
DC Biasing	±25V, I_1 = 400μA, I_1 = 200μA	±0.75V	±10V	±1.5V
Power Consumption	--	18.6μW	--	0.5 mW to 8.73mW

'--': means that specific data was not available in the concerned reference.

4. Comparison with Previously Known VCNR Circuits and Concluding Remarks

Compared to the previously known VCNR circuits which employ various analog building blocks such as op-amps as in [3,17,18], OMAs as in [27], and CFOAs as in [28,30] all of which would require a large number of MOSFETs when these would be implemented in CMOS technology (for instance, see [4]), the proposed VCNR requires a very small number of (only eight) MOSFTs (like the VCPR circuit of [10]) and is, therefore, highly suitable for implementation in CMOS technology.

On the other hand, a comparison of the proposed circuit with only transistor-level VCNRs (i.e. which do not require any additional active building blocks), such as those of [8,20,25], is shown in Table 1 from where it is revealed that performance-wise, the proposed VCNR circuit of Figure 1 exhibited good linearity, has good variable negative resistance range variable from -1.05kΩ to -300Ω and offers a good operational frequency range up to around 100 MHz with total power dissipation remaining between 0.5mW- 8.73mW while employing a very small number of (only 8) MOSFET.

It is expected that the proposed VCNR may find applications in realizing voltage-controlled attenuator/ amplifier, design of variable-bandwidth band-pass filters or Q-enhancement circuits.

In view of the requirement of *floating* voltage-controlled-resistance circuits in several applications, a worthwhile problem is to find a floating version of the proposed grounded VCNR circuit. This, however, is left for future work.

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