Square/Triangular Wave Generator Using Single DO-DVCC and Three Grounded Passive Components

Hung-Chun Chien^{*}

Department of Electronic Engineering, Jinwen University of Science and Technology, New Taipei City, Taiwan *Corresponding author: hcchien@just.edu.tw

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Abstract This study proposes a novel square/triangular wave generator based on a dual outputs differential voltage current conveyor (DO-DVCC). The proposed circuit uses one DO-DVCC combined with three grounded passive components. The presented scheme reveals a compact topology and can produce square/triangular waveform simultaneously. To verify their feasibility, commercially available ICs were used for implementing the prototype circuits. Experimental results revealed consistency with theoretical analyses.

Keywords: active RC circuit designs, dual outputs differential voltage current conveyor (DO-DVCC), square/triangular wave generator

1. Introduction

In early active RC circuit designs, operational amplifiers (OPAs) played a crucial role in implementing numerous signal generation/processing circuits [1]. Recently, active RC circuit designs using current-mode active devices were attractive because of their potential advantages over traditional OPAs, such as wider bandwidth. higher accuracy, and simplicity in implementation [2]. Current conveyor (CC) was the first introduced current-mode active device, which was reported in 1968 [3]. Since then, several novel active devices have been reported [4-10]. Square/triangular wave generators have wide applications in instrument, measurement, communication, and power conversion circuit control systems. For several years, the typical configuration of square/triangular generator was realized by using OPAs combined with external passive components [1]. In addition to OPA-based configuration, previous studies presented several implementations of square/triangular wave generators using different types of active devices [11-16]. For the reported square/triangular wave generators, one current tunable topology was designed using three operational transconductance amplifiers (OTAs) [12]. This circuit was built based on a current tunable Schmitt trigger connected to an OTA-C integrator. Although OTA-based wave generator exhibits the current tunable property, the transconductance gain of an OTA is a function of temperature. Thus, the wave generators implemented by OTA is sensitive with Moreover, environmental variation. а CC-based square/triangular wave generator was first introduced in 2000 [11]; and a recent study revealed a modified topology to enhance circuit performance and reduce the passive component counts [15]. A square/triangular wave generator using current feedback amplifiers (CFOAs) has

also been reported in [14]. In 2007 literature [13] presented an operational transresistance amplifier (OTRA) based scheme that featured switch-controllable operation. Recent research reports a DVCC-based topology constructed with two DVCCs and four passive This the components [16]. is first reported square/triangular wave generator built by DVCCs. The concept of the DVCC device was first introduced in 1989 [17]. Because the DVCC-based application circuits received considerable attention in recent years, this study proposes a novel circuit configuration to add to this list. Although DVCC-based square/triangular wave generator was discussed in a previous study [16], this paper presents a compact topology to implement a low cost design. To illustrate the novelty and difference of the proposed circuit, comparisons with other schemes are shown in Table 1. It should be noted that among the various solutions, the proposed circuit features the following benefits: 1) Fewer of active devices and passive components are used. 2) All passive components are grounded connections. 3) Higher operation frequency than OPA- and OTA-based designs. 4) Insensitive to the temperature.

2. DO-DVCC Fundamental and Its Realization

The circuit symbol of a DO-DVCC is shown in Figure 1, which includes two high-impedance voltage input terminals (Y_1 and Y_2), one low-impedance current output terminal (X), and a couple of high-impedance current output terminals (Z+). Its terminal relationships are defined by (1), where the X terminal voltage follows the voltage difference of terminals Y_1 and Y_2 , and a current injected into the terminal X is replicated to the terminal Z+ of the same flow direction. An ideal DO-DVCC exhibits zero input resistance at the terminal X, and

infinite resistances at $Y_1 \mbox{ and } Y_2$ terminals, as well as at the terminal Z+.

Table 1. Comparisons amo	ong various	square/triangular	wave
generators			

Circuit topology	Component numbers	Passive component types	Electronically tunable/ Insensitive to temperature	Highest operation frequency
OPA-based [1]	OPA × 2 Resistor × 3 Capacitor × 1	Floating	No/ Yes	Tens of kHz
CC-based [11]	$\begin{array}{c} \text{CCII} \times 2\\ \text{Resistor} \times 3\\ \text{Capacitor} \times 2 \end{array}$	Only one floating	No/ Yes	Hundreds of kHz
CC-based [15]	$\begin{array}{c} \text{CCII} \times 2\\ \text{Resistor} \times 3\\ \text{Capacitor} \times 1 \end{array}$	Floating	No/ Yes	Hundreds of kHz
CFOA- based [14]	CFOA × 2 Resistor × 4 Capacitor × 1	Only one grounded	No/ Yes	Hundreds of kHz
OTRA- based [13]	$OTRA \times 2$ Resistor $\times 3$ Capacitor $\times 1$ Switch $\times 3$	Floating	Yes/ Yes	Hundreds of kHz
OTA-based [12]	OTA × 3 Resistor × 2 Capacitor × 1	Grounded	Yes/ No	Tens of kHz
DVCC- based [16]	$\frac{\text{DVCC} \times 2}{\text{Resistor} \times 3}$ Capacitor × 1	Grounded	No/Yes	Hundreds of kHz
DO-DVCC- based (Proposed)	$\begin{array}{c} \text{DO-DVCC} \times 1 \\ \text{Resistor} \times 2 \\ \text{Capacitor} \times 1 \end{array}$	Grounded	No/ Yes	Hundreds of kHz



Figure 1. Circuit symbol of a DO-DVCC

$$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Z1} \\ I_{Z2} \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_{Z1} \\ V_{Z2} \end{bmatrix}$$
(1)

To evaluate the effectiveness of the proposed circuit, a implementation of DO-DVCC practical using commercially available IC (AD844AN) is shown in Figure 2. The AD844AN has the following properties: the voltage on the non-inverting input terminal is transferred to the inverting input terminal, and the current into the inverting input terminal is replicated to the terminal T_z . In this manner, the non-inverting input terminals of the first and second AD844ANs were used to simulate the two high-impedance inputs, Y_1 and Y_2 , of a DO-DVCC, as shown in Figure 2. To produce a terminal voltage V_x proportional to the difference of Y_1 and Y_2 voltages, a resistor R_a was settled between the inverting input terminals of the first and second AD844ANs, and the T_z node of the first AD844AN was subsequently connected to the non-inverting input terminal of the third AD844AN with a grounded resistor R_b . The fourth and fifth AD844ANs and resistors (R_c , R_d , and R_e) perform the function of the dual output currents (I_{z1} , and I_{z2}). As shown in Figure 2, the following relationships can be obtained:



Figure 2. DO-DVCC constructed using commercially available ICs

$$V_{Y1} = V_{1+} = V_{1-} \tag{2}$$

$$V_{Y2} = V_{2+} = V_{2-} \tag{3}$$

$$I_{Y1} = I_{Y2} = 0 (4)$$

$$I_{T1} = I_{2-} = \frac{V_{1-} - V_{2-}}{R_a} = \frac{V_{Y1} - V_{Y2}}{R_a}$$
(5)

$$I_X = I_{3-} = I_{T3} \tag{6}$$

$$V_X = V_{3-} = V_{3+} = I_{T1} \times R_b = \frac{R_b}{R_a} (V_{Y1} - V_{Y2})$$
(7)

$$V_{4+} = V_{4-} = V_{5+} = V_{5-} = I_{T3} \times R_c = I_X \times R_c$$
(8)

$$I_{Z1} = I_{T4} = I_{4-} = \frac{V_{4-}}{R_d} = \frac{R_c}{R_d} I_X$$
(9)

$$I_{Z2} = I_{T5} = I_{5-} = \frac{V_{5-}}{R_e} = \frac{R_c}{R_e} I_X \tag{10}$$

Therefore, if $R_a = R_b$ and $R_c = R_d = R_e$, the terminal behavior of an ideal DO-DVCC can be precisely fulfilled. Because the AD844AN IC is widely used to implement a variety of analog circuits, the realization shown in Figure 2 is capable of providing a viable method to implement a DO-DVCC in practice.

3. Circuit Descriptions and Operations

Figure 3 shows the circuit diagram and its output waveforms associated with the proposed square/triangular wave generator. Only one DO-DVCC and three grounded passive components are required. The Y_1 -Z+ connection in conjunction with the resistor R_2 forms a positive-feedback path, and thus, the DO-DVCC saturates with its voltage levels either at the positive saturation level V_o^+ or at the negative saturation level V_o^- at output V_{o1} ($V_o^+ = |V_o^-|$). In Figure 3(b), V_o^+ and V_{TL} represent the upper and lower threshold levels, respectively. The circuit operation can be divided into two modes (on-duty cycle T_1 , and off-duty cycle T_2). In the on-duty cycle, V_{o1} is at the positive saturation level V_o^+ in the beginning. To establish that the

voltage level of V_{o1} is V_{o}^{+} from the beginning, the current I_X must have a stronger positive charge than I_Z . Let R_2 be greater than R_1 to achieve this requirement. At this time, the capacitor C is charged, causing V_{o2} to increase linearly. The increasing rate of V_{o2} and the expressions of currents I_X and I_Z are determined in (11) to (13). This state continues until V_{o2} reaches the upper threshold level V_{TH} . Subsequently, the circuit leaves on–duty cycle operation into the off-duty cycle.



Figure 3. (a) Circuit diagram of the proposed DO-DVCC-based square/triangular wave generator, and (b) its output waveforms



$$I_X = \frac{V_{o1} - V_{o2}}{R_1} = \frac{V_o^+ - V_{o2}}{R_1}$$
(12)

$$I_Z = I_{Z1} = I_{Z2} = \frac{V_{o1}}{R_2} = \frac{V_o^+}{R_2}$$
(13)

In the off-duty cycle, V_{o1} is held at V_o^- , and V_{o2} starts to decrease linearly. At the end of this discharging state, V_{o2} reaches V_{TL} . Subsequently, the operation returns to on-duty cycle mode. The decreasing rate of V_{o2} and the currents I_X and I_Z in this state are expressed in (14) to (16).

$$\frac{dV_{o2}(t)}{dt} = \frac{V_{o1}}{R_2C} = \frac{-V_o^+}{R_2C} = \frac{V_{TL} - V_{TH}}{T_2}$$
(14)

$$I_X = \frac{V_{o1} - V_{o2}}{R_1} = \frac{-V_o^+ - V_{o2}}{R_1}$$
(15)

$$I_Z = I_{Z1} = I_{Z2} = \frac{V_{o1}}{R_2} = \frac{-V_o^+}{R_2}$$
(16)

Using (12), (13), (15), and (16), and setting $I_X = I_Z$, V_{TH} , and V_{TL} can be derived in (17).

$$V_{TH} = -V_{TL} = \left(1 - \frac{R_1}{R_2}\right) V_o^+$$
(17)

From (11), (14), and (17), the oscillating frequency is provided by

$$f = \frac{1}{T_1 + T_2} = \frac{1}{4R_2C\left(1 - \frac{R_1}{R_2}\right)}$$
(18)



Figure 4. Non-ideal circuit model of the applied DO-DVCC

4. Non-ideal Effects of the Proposed Circuit

From datasheet [18], a practical AD844AN IC can be modeled as a positive current conveyor (CC+) cascading a voltage buffer with finite parasitic resistances (R_x , R_y , and R_z) and non-ideal voltage and current tracking gains. A more sophisticated non-ideal model of the applied DO-DVCC (Figure 2) is shown in Figure 4. Parasitic R_x was on the order of several tens of ohms, whereas R_y and R_z were in the range of a few mega ohms. α denotes the nonideal voltage tracking gain from the non-inverting node to the inverting node, and β represents the non-ideal current tracking gain at T_z with respect to the inverting node of CC+. From the AD844AN datasheet, the standard values of these parameters can be acquired as $\alpha = 0.99$, $\beta = 0.98$, $R_x = 50 \ \Omega$, $R_y = 10 \ M\Omega$, and $R_z = 3 \ M\Omega$. The resulting expressions of the related currents are included in Figure 4.

Considering the non-ideal DVCC model, for the square/triangular wave generator (Figure 3), the expressions of the increasing/decreasing rate of V_{o2} and the currents I_X and I_Z are modified in (19) to (21).

$$\frac{dV_{o2}(t)}{dt} = \frac{V_{o1}}{\left(\frac{R_2}{R_y}\right)} = \frac{V_{TH} - V_{TL}}{T_1} = \frac{V_{TL} - V_{TH}}{T_2}$$
(19)
$$V_2 = \frac{\alpha^2 \beta \left(\frac{R_b}{R_y}\right)}{R_y} = \frac{V_{TL} - V_{TH}}{T_2}$$
(19)

$$I_X = \frac{V_{3-}}{R_1 + R_x} = \frac{\alpha \, P\left(R_b + R_y + R_z\right)}{(R_1 + R_x)(R_a + 2R_x)} (V_{o1} - V_{o2}) \tag{20}$$

$$I_{Z} = I_{Z1} = I_{Z2} = \frac{V_{o1}}{R_{2} / / R_{y} / / R_{z}} = \frac{\alpha \beta^{2} \left(\frac{R_{c} / / R_{z} / / \frac{1}{2} R_{y}}{R_{d} + R_{x}} \right)}{R_{d} + R_{x}} I_{X}$$
(21)

Setting $I_x = I_z$ and substituting the saturation levels of V_{o1} into (19), (20), and (21), the modified upper and lower threshold levels, V_{TH} and V_{TL} , can be derived as in (22). The oscillating frequency is determined in (23).

$$V_{TH} = -V_{TL} = \left(1 - \frac{R_a}{(\alpha\beta)^3 R_b} \frac{R_1}{R_2}\right) V_o^+$$
(22)

$$f = \frac{1}{T_1 + T_2} = \frac{1}{4R_2C\left(1 - \frac{R_a}{(\alpha\beta)^3 R_b} \frac{R_1}{R_2}\right)}$$
(23)

In (22), and (23), the following conditions are applied: $R_1 >> R_x$, $R_2 << (R_y//R_z)$, $R_3 << R_z$, $R_a >> R_x$, $R_b << (R_y//R_z)$, $R_c << R_y$, $R_c << R_z$, $R_d >> R_x$, and $R_c = R_d = R_e$. From (22) and (23), the non-ideal voltage and current tracking gains slightly influenced the threshold levels and oscillating frequency using the presented circuit. However, this slight deviation can be compensated for by tuning the ratio of R_a/R_b . Thus, if (24) is satisfied, the influence of these non-ideal effects would be nearly disregarded.

$$R_a = \left(\alpha\beta\right)^3 R_b \tag{24}$$

5. Design Procedures and Experimental Results

Several experimental tests are presented to demonstrate the theoretical analysis of the proposed circuit. To demonstrate the validity of the theoretical analysis, a prototype circuit was built using AD844AN ICs combined with discrete passive components for experimental testing.

All experiments were performed at supply voltages of ±10 V with saturation levels $V_o^+ = -V_o^- = 9.6V$. Equations (22), (23), and (24) are useful to facilitate the design procedures. First, (24) was applied to fulfill the function of an ideal DO-DVCC. A proper value of R_b was first selected, and parameters α and β were obtained from the AD844AN datasheet. Ra can subsequently be determined. For the proposed square/triangular wave generator (Figure 3), a suitable ratio R_1/R_2 is chosen, and an oscillating frequency is specified. The capacitor C is arbitrarily determined. Subsequently, R_2 and R_1 are obtained from (23). Based on the design procedures, substituting the parameters $\alpha = 0.99$ and $\beta = 0.98$ into (24) enables calculation of $R_a/R_b = 0.91$. To satisfy the conditions $R_a >> R_x$, and $R_b << (R_v // R_z)$, $R_a = 9.1 \ k\Omega$ and $R_b = 10$ $k\Omega$ were selected. $R_c = R_d = R_e = 10 \ k\Omega$ were used to fulfill $R_c \ll R_v$, $R_c \ll R_z$, $R_d \gg R_x$, and $R_c = R_d = R_e$. For the proposed square/triangular wave generator, the oscillating frequency was specified as f = 10 kHz; a resistor ratio $R_1/R_2 = 0.5$ was set. Subsequently, C was chosen as 10nF. From (23), $R_2 = 5k\Omega$ was considerably smaller than $R_z //R_y$, and $R_1 = 2.5k\Omega$ was considerably larger than R_x. Figure 5 shows the experimental result of output waveforms for the proposed square/triangular wave generator. It can be concluded that the oscillating frequency for the experimental result was close to the design value f = 10kHz. To investigate the operations for varying oscillating frequencies, the most convenient method was to use a different capacitor, leaving R_1 and R_2 unchanged. Figure 6 shows the experimental results with f = 100 kHz (C = 1 nF), f = 500 kHz (C = 200 pF), and f = 800kHz (C = 125pF). Because the slew rate of the output voltage for the AD844AN IC and the prototype circuit was implemented on a breadboard, the highest applicable oscillating frequency of the proposed square/triangular wave generator was demonstrated only at approximately several hundred kilohertz, as shown in Figure 6. Obvious distorted output waveforms occurred with an oscillating frequency of 800kHz. The highest operating frequency of the square/triangular wave generators consisting of OPA, and OTA were also verified through the experiment, and were below 100kHz.



Figure 5. Experimental results of output waveforms with f = 10 kHz for the proposed square/triangular wave generator



Figure 6. Experimental results of output waveforms with (a) f = 100 kHz, (b) f = 500 kHz, (c) f = 800 kHz for the proposed square/triangular wave generator

6. Conclusions

This study presents a novel DO-DVCC-based application circuit (DO-DVCC-based square/triangular wave generator). The circuit topology is simple since only one DO-DVCC and a few passive components are utilized. The operation principle of the proposed circuit is described, and the non-ideal effect on the presented circuit is also discussed. The effectiveness of the circuit was verified through experimental tests. Experimental results are consistent with the theoretical analysis. The presented circuits can be widely applied in instrumentation, measurement, communication, and signal processing systems.

References

- Franco, S, Design with Operation Amplifiers and Analog Integrated Circuits, 3th ed, McGraw-Hall, New York, 2002.
- [2] Toumazou, C., Lidegy, F. J. and Haigh, D, Analog IC Design: The Current-Mode Approach, Peter Peregrinus Press, U.K, 1990.
- [3] Smith, K. C. and Sedra, A. S, "The current conveyor: a new circuit building block," Proceedings of IEEE, 56 (8). 1368-1369. Aug.1968.
- [4] Acar, C. and Ozoguz, S, "A new versatile building block: current differencing buffered amplifier suitable for analog signal processing filter," Microelectron. J., 30 (2). 157-160. Feb.1999.
- [5] Salama, K. N. and Soliman, A. M, "CMOS operational transresistance amplifier for analog signal processing," Microelectron. J., 30 (3). 235-245. Mar.1999.
- [6] Alzaher, H. and Ismail, M, "A CMOS fully balanced differential difference amplifier and its applications," IEEE Trans. Circuits Syst. II, 48 (6). 614-620. Jun.2001.
- [7] Barthelemy, H. and Fabre, A, "A second generation current controlled conveyor with negative intrinsic resistance," IEEE Trans. Circuits Syst. I, 49 (1). 63-65. Jan.2002.
- [8] Ghallab, Y. H., Badawy, K. K. V. and Maundy, B. J, "A novel current-mode instrumentation amplifier based on operational floating current conveyor," IEEE Transactions on Instrumentation and Measurement, 54 (5). 1941-1949. Oct.2005.
- [9] Maundy, B. J., Sarkar, A. R. and Gift, S. J, "A new design topology for low-voltage CMOS current feedback amplifiers," IEEE Trans. Circuits Syst. II, 53 (1). 34-38. Jan.2006.
- [10] Siripruchyanun, M. and Jaikla, W, "A current-mode analog multiplier/divider based on CCCDTA," Int. J. Electron. Commun., 62 (3). 223-227. Mar.2008.
- [11] Almashary, B. and Alhokail, H, "Current-mode triangular wave generator using CCIIs," Microelectron. J., 31 (4). 239-243. Apr.2000.
- [12] Chung, W. S., Kim, H., Cha, H. W. and Kim, H. J, "Triangular/square-wave generator with independently controllable frequency and amplitude," IEEE Trans. Instrum. Meas., 54 (1). 105-109. Feb.2005.
- [13] Lo, Y. K. and Chien, H. C, "Switch-controllable OTRA-based square/triangular waveform generator," IEEE Trans. Circuits Syst. II, 54 (12). 1110-1114. Dec.2007.
- [14] Saque, A. S., Hossain, M. M., Davis, W. A., Russell, H. T. and Carter, R. L, "Design of sinusoidal, triangular, and square wave generator using current feedback amplifier (CFOA)," IEEE Region 5 Conference, 1-5. Apr.2008.
- [15] Pal, D., Srinivasulu, A., Pal, B. B., Demosthenous, A. and Das, B. N, "Current conveyor-based square/triangular waveform generators with improved linearity," IEEE Trans. Instrum. Meas., 58 (7). 2174-2180. Jul.2009.
- [16] Minaei, S. and Yuce, E, "A simple schmitt trigger circuit with grounded passive elements and its application to square/triangular wave generator," Ciruits, Systems, and Signal Processing, 31 (3). 877-888. Jun.2012.
- [17] Pal, K, "Modified current conveyors and their applications," Microelectron. J., 20 (3). 37-40. Aug.1989.
- [18] Analog Devices AD844 datasheet.