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Review of Leakage Power Reduction in CMOS Circuits

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Abstract Recent Technological advances in Wireless Communication has shown the convergence of terminals and networks that support multimedia and real-time applications. This obviously puts an immense pressure on battery of any mobile device. The CMOS has been the leading technology in today's world of mobile communication due to its low power consumption. Reduction of leakage power in CMOS has been the research interest for the last couple of years. In CMOS integrated circuit design there is an important trade-off between technology scaling and static power consumption. In today's CMOS technology the leakage power consumption plays a significant role. As we approaching to nano-scale design the total chip power consumption becomes dependent on leakage power. Increasing the battery life in mobile wireless communication and mobile computing and similar other applications is the topic of research now-a days... Further, since the leakage of battery exists even when devices are in idle state makes leakage power loss most critical in CMOS VLSI circuits. Many techniques have been evolved to tackle the problem and its still in progress. This paper mainly focuses on the review of various works done in this field till today's date. Further a review of recent work done on a new technique LSSR (Lector Stack State Retention Technique) is discussed in the paper.

Keywords: *CMOS, Leakage power, VLSI circuits, multimedia applications, Static power, Nano Scale, LSSR*

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1. Introduction

The rapid growth in semiconductor technology through the use of deep-submicron processes has led the feature sizes to be shrinking; thereby integrating extremely complex functionality on a single chip. In the ever increasing market of mobile hand-held devices used all over the world today, the battery-powered electronic system forms the backbone. To maximize the battery life, the tremendous computational capacity of portable devices such as notebook computers, personal communication devices (mobile phones, pocket PCs, PDAs), hearing aids and implantable pacemakers has to be realized with very low power requirements.

The power dissipation has become a very critical design metric due to device miniaturization and rapid growth towards wireless communication. The longer the battery lasts; the better is the device [13]. The power dissipation has not diminished even with the scaling down of the supply voltage. The problem of heat removal and power dissipation is getting worse as the magnitude of power per unit area has kept growing. There is a little help from advanced cooling and packaging strategies the rapid increase in power consumption of present day chips. Also, the cost associated with the packaging and the cooling of such devices is becoming prohibitive. In addition to cost, the issue of reliability is a major concern. It is already reported that Component failure rate roughly doubles for every 10°C increase in operating temperature. Following Moore's law, with the on-chip devices doubling every two years, minimizing the power consumption has become currently an extremely challenging area of research. Leakage power of a CMOS transistor depends on gate length and oxide layer thickness. To decrease the dynamic power, the supply voltage is decreased which leads to the performance degradation. To increase the operating speed the device, the threshold voltage should also be scaled down along with the supply voltage, which results in exponential increase in the sub-threshold leakage current, thereby increase in the static power dissipation. The main components of leakage current in a MOS transistor are shown in Figure 1.

With the increase in the leakage current more and more, as will be seen that it becomes proportional to the total power dissipation as given by following equation.

$$P_{leak} = I_{leak} * V_{dd} \quad (1)$$

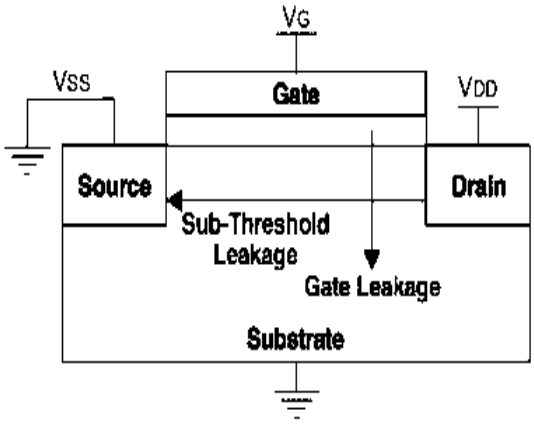

Figure 1. Static CMOS Leakage Power Sources [21]

In today's world there is a huge demand for minimizing the dynamic power dissipation and scaling down the supply voltage by pushing the circuits design towards ever-shortening channel lengths in CMOS technology [19]. To maintain the circuit speed, the transistor threshold voltages must also be scaled down [1]. This can be easily seen from the first-order propagation delay equation of a transistor given by following equation.

$$\tau = \frac{C\ Vdd}{(Vdd - Vt)^x} \quad (2)$$

Where C is the load capacitance, Vt is the threshold voltage; x (which is greater than 1 but less than 2) models the short channel effect. The sub threshold leakage current exponentially increases as Vt is reduced. This principle of sub threshold current is followed by most of the techniques for low leakage power [6].

It has been shown that as the technology scales down below 100nm which is the shrinking of feature size of transistor, the channel length decreases, thereby increasing the amount of leakage power in the total power dissipated. As we can see as the technology is moving towards lower nanotechnology the sub-threshold leakage increases thereby affecting the battery life. Thus there were various technique developed to deal with this problems. The various techniques will be discussed in the next section along with their drawbacks.

2. Related Works Done

Many techniques have been come into existence to overcome the leakage power problem in the nano-scale technology, but those techniques have tradeoff between area, delay and also active power. Some of those techniques are as described in this section.

2.1. Dual Vt and MTCMOS

This was the earliest suggested technique to reduce the leakage power. As stated in [1,7] Dual VT technique is a variation in MTCMOS, in which the gates in the critical path use low-threshold transistors and high-threshold transistors for gates in non-critical path. According to the authors both the methods requires additional mask layers for each value of Vt in fabrication, which is a complicated task depositing two different oxides thickness, hence making the fabrication process complex. Moreover the techniques also suffer from turning-on latency i.e., the idle of circuit cannot be used immediately after reactivated since sometime is needed to return to normal operating condition. The latency is typically a few cycles for former method, and for Dual technology, is much higher. When the circuit is active, these techniques are not effective in controlling the leakage power.

2.2. Sleep Mode Approach

This method was developed to overcome the disadvantages of the dual Vt and MTCMOS technique. According to [8] it is one of the most commonly known traditional approaches for sub threshold leakage power reduction is the sleep approach. In this sleep approach, additional transistors (sleep transistors) are inserted in between the power supply and ground.

As explained in [1] in this technique an additional "sleep" PMOS transistor is placed between VDD and the pull-up network of a circuit and an additional "sleep" NMOS transistor is placed between the pull-down network of the circuits and GND [6]. These sleep transistors turn off the circuit by cutting off the power rails. The sleep transistors are turned on when the circuit is active and provide very low resistance in the conduction path so that circuit's performance will not get affected due to these additional transistors. During the standby mode the leakage power is reduced in the circuit by making transistors turned off which introduces large resistance in the conduction path. Thus leakage power can be reduced effectively by switching off the power source. These types of techniques are also called gated-VDD and gated- GND.

2.3. Stack Approach

The sleep technique though proved to be better than dual Vt and MTCMOS technique but however could not give a satisfying result in reducing the leakage power. This led to the authors in [8] to design a new better circuit and in this race they suggested a new technique called the stack technique which forces a stack effect by breaking down an existing transistor into two half size transistors. The authors suggested the circuit as shown in Figure 2.

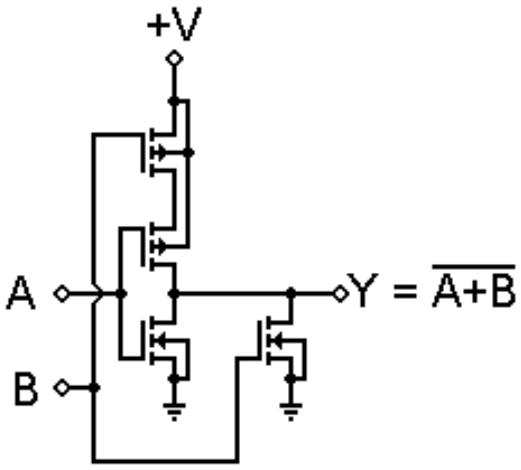

Figure 2. Stack mode approach using 2 input NOR gate [22]

The authors in their work [1] explained the concepts behind the design suggested. It is shown that induced

reverse bias between the two transistors results when the two transistors are turned off together resulting in sub-threshold leakage current reduction. But the disadvantage is increase delay significantly between divided transistors which could limit the usefulness of the approach.

2.4. Sleepy Keeper Approach

In [11,13] the authors have explained the various problems faced by conventional CMOS circuit. They stated that the basic problem with traditional CMOS is that the transistors are used only in their most efficient, and naturally inverting, i.e., PMOS transistors are connect to VDD and the NMOS transistors are connect to GND. It is a well known fact that the PMOS transistors are not efficient at passing GND and that the NMOS transistors are not efficient at passing VDD. However, to maintain a value of '1' in sleep mode, given that the '1' value has already been calculated, the sleepy keeper approach uses this output value of '1' and an NMOS transistor connected to VDD to maintain output value equal to '1' when in sleep mode. To tackle this problem the authors suggested a new design using sleepy keeper approach in which an additional single NMOS transistor placed in parallel to the pull-up sleep transistor connects VDD to the pull-up network. When in sleep mode, this NMOS transistor is the only source of VDD to the pull-up network since the sleep transistor is off. An additional single PMOS transistor placed in parallel to the pull-down sleep transistor is the only source of GND to the pull-down network. The suggested circuit can be seen in Figure 3.

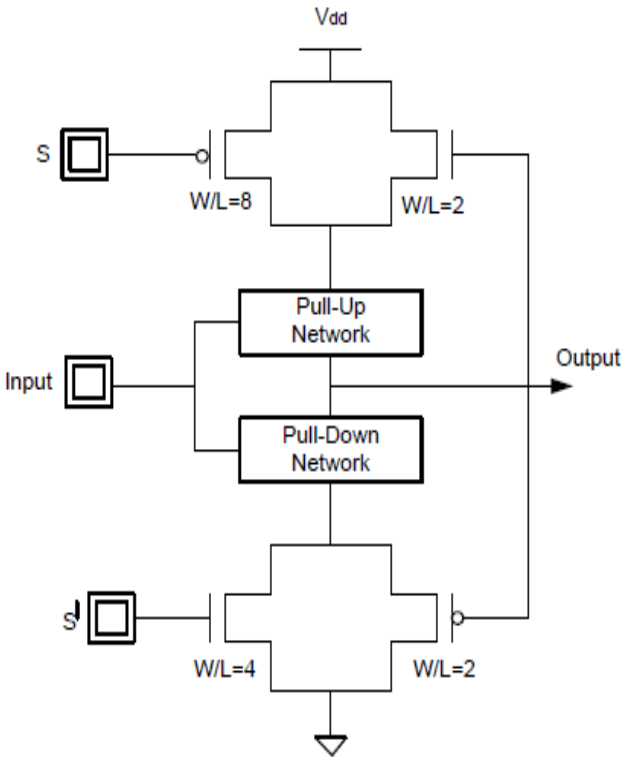

Figure 3. Sleepy Keeper circuit [11,23]

However it was reported that major disadvantage faced by this technique was the reduction of power by very less percentage which was not able to fulfill the current demands of present requirement of the VLSI designed circuits.

2.5. LECTOR Technique

This is one of the low power retention techniques as stated in [1]. The authors suggested a CMOS circuit in which two extra Leakage Control Transistors (a P-type and an N-type) is inserted within the gate, in which the gate terminal of each Leakage Control Transistor is controlled by the source of the other. The circuit can be viewed in Figure 4.

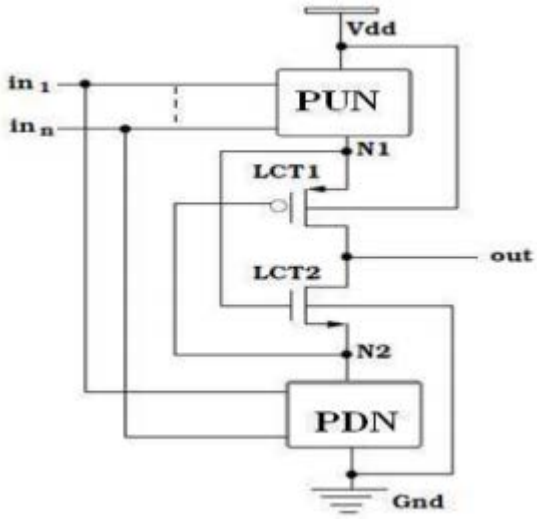

Figure 4. LECTOR circuit design [1,8]

The basic idea behind their approach was for reduction of leakage power is the effective stacking of transistors in the path from supply voltage to ground. The authors in [8,10,16], and [17] made an observation that "a state with more than one transistor OFF in a path from supply voltage to ground is far less leaky than a state with only one transistor OFF in any supply to ground path." In their method they introduced two leakage control transistors (LCTs) in each CMOS gate such that one of the LCTs is near its cutoff region of operation. They illustrated that their Leakage Control Transistor technique (LECTOR) with the case of a NAND gate .A CMOS NAND gate with the addition of two leakage control transistors.

3. Motivation

It is seen that overall leakage power is mainly due to sub-threshold leakage [8]. In addition, gate-oxide leakage is another possible contributor to leakage power. A possible solution widely studied is the potential use of high-k (high dielectric constant) gate insulators [9]. Again the aim of this paper is to review the reduction of the sub threshold leakage component of static power consumption by various methods implemented till date.

It was seen that there was a reduction in magnitude sub threshold leakage power with application of dual threshold voltage (Vth) techniques, along with the sleep and sleepy stack approaches [7]. As per the reviews the major advantage of the sleepy stack approach over the sleep approaches is that the sleepy stack approach saves exact logic state. But the sleepy stack approach comes with a demerit that each transistor in the original, base case, traditional CMOS design results in three transistors in the sleepy stack equivalent [11]. The goal of this paper is to give the review of the latest approach to achieve large

reduction of leakage power in CMOS circuits. The new approach is called LSSR (Lector Stack State Retention Technique) as given by [1].

4. LSSR (Lector Stack State Retention Technique)

The main aim of this paper is to review the works being done on this approach to achieve low power in VLSI circuits. The authors in [1] introduced this approach .In order to achieve low power they formed this new circuit design by combining two previously done approaches namely LECTOR approach and Forced stack approach. Since it combines the two above mentioned techniques it has the features of both the approaches and thus is much beneficial than the previous works done.

The authors in [1] have proposed the circuit by introducing two gated leakage transistors between pull up and pull down networks with high threshold voltage, and then stack effect is added to pull up and pull down networks by dividing each transistor in to half size transistors.

As per the works being in progress the authors believe that this new technique LSSR can be proved to be much better than the earlier works done as according to [1,10] LSSR which can achieve better leakage reduction by maintaining exact logic state(state retention) than the other techniques.

5. Conclusion

The main of this paper was to give a review of the various steps taken towards the reduction of the leakage power for VLSI designs. A major thrust towards the low power design of CMOS is actually due to recent technological advances in wireless communication because the usable time of a mobile device is heavily restricted by its battery life. With the growing complexity of mobile devices, such as with a digital camera, multimedia services, Video Conferencing, global positioning system (GPS) etc are the features which make the battery power problem more challenging.

To solve the problem faced various works have been implemented and still technicians are working on this field. However through this paper we get to know the advantages and disadvantages of various works done .We conclude that LECTOR and the new approach LSSR circuit may lead to much large reduction of leakage power than the stack and sleep approaches. Finally it is concluded that the optimized layout will also play an important role in reducing the leakages.

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