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DVCC Based K.H.N. Biquadratic Analog Filter with Digitally Controlled Variations

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Abstract In this paper, a digitally controlled single input multi output current-mode K.H.N. Biquad Filter is presented. The filter circuit is composed of three DVCCs together with four grounded resistors and two grounded capacitors. The digital control is incorporated using a current-summing network (CSN). Tuning of resonant frequency is carried out by 3–bit digital control word. Block by block replacement has been done to observe the change in the relationship between resonant frequency of the band-pass filter with the control word. The filter circuit showed three different variations when the DVCC blocks were replaced (one by one) with 3-bit DC-DVCC blocks. PSPICE simulations using TSMC 0.25 micron CMOS technology have been performed to validate the theoretical results.

Keywords: *Current-mode, Differential Voltage Current Conveyor (DVCC), multifunctional filter, digitally controlled DVCC (DC-DVCC), Cut off frequency, K.H.N. Biquad filter*

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1. Introduction

In the recent times the current mode filters have gained utility in various signal processing applications. These filters have revolutionized the modern day signal processing and have replaced their voltage mode counterparts in several of applications.

Moreover filters which could provide simultaneous realization of the basic filter functions have proved themselves useful in various applications which include touch-tone telephone tone decoder, phase-locked loop FM stereo demodulator and crossover network used in a three-way high-fidelity loudspeaker.

With the inception of Current Conveyors (CC), the filter design has reached a new height and various variants of CC have also gained attraction [1-10]. Various digitally controlled filters have been proposed and realized in the recent times. In [11] H.P. Chen and S.S. Shen presented a DVCC based Universal capacitor grounded voltage mode filter which realized all the five generic filter responses simultaneously. In [12] H. P. Chen presented tunable current mode universal filter, the high output impedance of this filter enable easy cascading in current-mode operation also in different modes of operation it could realize different filter responses simultaneously. Two years back I. A. Khan and A. M. Nahhas presented a CCII based reconfigurable first order multifunction filter whose frequency could be changed with a digital control word [13].

In this paper, the circuit proposed in [14] by Muhammed A. Ibrahim, Shahram Minaei and Hakan Kuntman, has been used to design and implement a digitally controlled current-mode K.H.N. biquad. Using grounded capacitors, the circuit becomes suitable for integration as the grounded capacitor circuit can compensate for the stray capacitances at the respective nodes. PSPICE simulations of the CMOS based programmable filter are performed to demonstrate results.

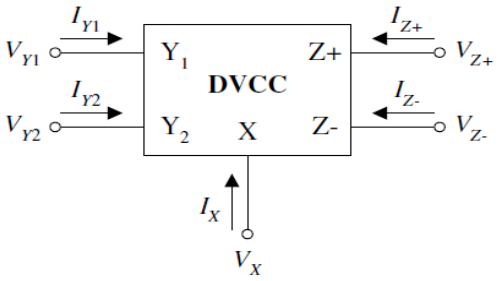

Figure 1. Symbol representing the dual output DVCC [15]

2. DVCC

DVCC is a five-terminal active analog building block illustrated in Figure 1, with terminal characteristics described by the following matrix equation [15].

$$\begin{pmatrix} I_{Y1} \\ I_{Y2} \\ V_X \\ I_{Z+} \\ I_{Z-} \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 \end{pmatrix} \begin{pmatrix} V_{Y1} \\ V_{Y2} \\ I_X \\ V_{Z+} \\ V_{Z-} \end{pmatrix} \quad (1)$$

DVCC exhibits negligible (ideally zero) input resistance at terminal X, and very high (ideally infinite) resistance at both Y terminals as well as the Z terminal. The output current follows the input current direction with both currents flowing either into or out of the device. The CMOS implementation of DVCC is as shown in Figure 2.

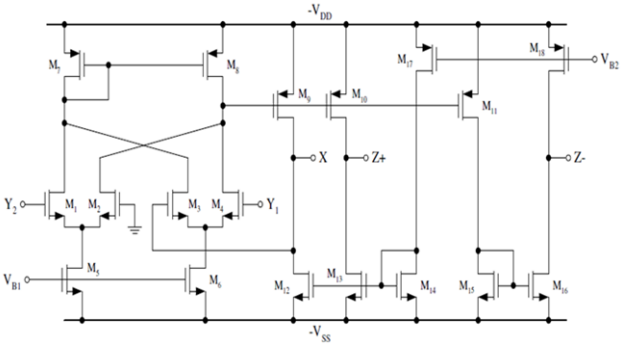

Figure 2. CMOS realization of the dual-output DVCC [15]

IMPLEMENTATION OF KHN BIQUAD

The implemented KHN biquad is illustrated in Figure 3. The analysis of the circuit yields the following equations (2), (3) and (4).

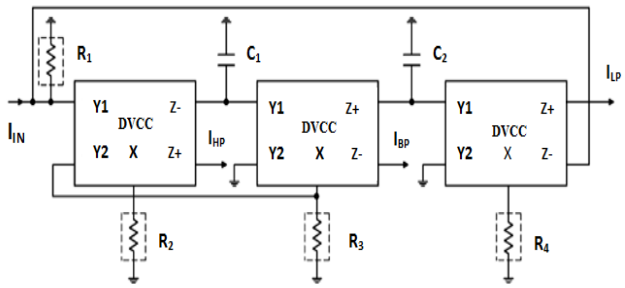

Figure 3. K.H.N. Biquad Filter Realization [14]

$$\frac{I_{BP}}{I_{IN}} = \frac{s\frac{R_1}{R_2R_3C_1}}{s^2 + s\left(\frac{1}{R_2C_1}\right) + \frac{R_1}{R_2R_3R_4C_1C_2}} \quad (2)$$

$$\frac{I_{HP}}{I_{IN}} = \frac{s^2\frac{R_1}{R_2}}{s^2 + s\left(\frac{1}{R_2C_1}\right) + \frac{R_1}{R_2R_3R_4C_1C_2}} \quad (3)$$

$$\frac{I_{LP}}{I_{IN}} = \frac{\frac{R_1}{R_2R_3R_4C_1C_2}}{s^2 + s\left(\frac{1}{R_2C_1}\right) + \frac{R_1}{R_2R_3R_4C_1C_2}} \quad (4)$$

The resonant angular frequency ω_o, and the quality factor, Q, are given by (5) and (6) respectively.

$$= \sqrt{\frac{R_1}{R_2R_3R_4C_1C_2}} \quad (5)$$

$$Q = \sqrt{\frac{R_1C_1R_2}{R_3R_4C_2}} \quad (6)$$

We can see that lowpass, bandpass and highpass functions can be simultaneously realized without changing the topology.

In simulations, using PSPICE the DVCC was realized by the CMOS implementation shown in Figure 2 using TSMC 0.25-µm process parameters. The aspect ratios of the CMOS transistors of the DVCC are presented in Table I. The supply voltages were taken as, $V_{DD} = -V_{SS} = 2$ V and the biasing voltages were assigned values, $V_{B1} = -1.32$ V and $V_{B2} = +0.7$ V. The circuit was designed for $f_o = \omega_o/2\pi = 100$ kHz and $Q = 0.707$ by choosing $R_1 = R_2 = R_3 = R_4 = 1$ kΩ and $C_2 = 2\ C_1 = 1.125$ nF. The responses of the multifunctional filter are shown in Figure 4 (a) and Figure 4 (b). The results are in full conformity with the theoretical analysis.

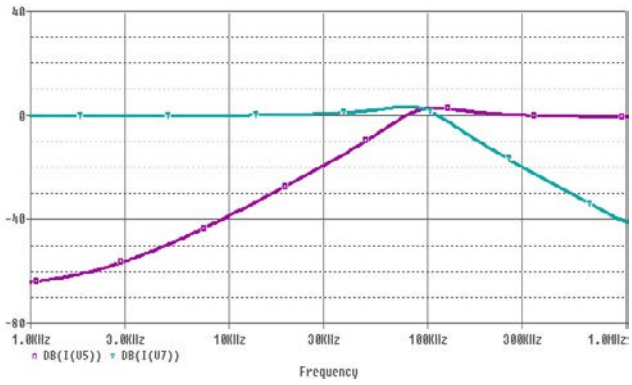

Figure 4 (a). Simulated Lowpass and Highpass responses

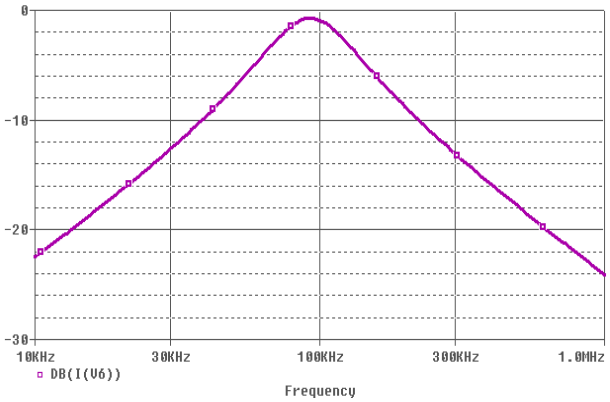

Figure 4 (b). Simulated Bandpass response

Table 1. Aspect ratios of the cmos transistors of the dvcc [15]

Transistors	W (µm)	L (µm)
M_1-M_4	1	0.8
M_5-M_6	24.2	0.8
M_7-M_8	6.8	0.8
M_9-M_{11}, M_{17}	18.6	0.6
M_{12}-M_{14}	25	0.8
M_{15}	19.6	0.8
M_{16}	18	0.8
M_{18}	20	0.6

3. DC-DVCC

To introduce the programmability in the multifunctional filter we have used a digitally controlled DVCC (DC-

DVCC) shown in Figure 5. The modified terminal characteristics for the same are as follows

$$\begin{pmatrix} I_{Y1} \\ I_{Y2} \\ V_X \\ I_{Z+} \\ I_{Z-} \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & k & 0 & 0 \\ 0 & 0 & -k & 0 & 0 \end{pmatrix} \begin{pmatrix} V_{Y1} \\ V_{Y2} \\ I_X \\ V_{Z+} \\ V_{Z-} \end{pmatrix} \quad (7)$$

Where:

$$k = \frac{I_Z}{I_X} \quad (8)$$

For obtaining the digital control in the DVCC current summing networks (CSNs) are employed at the Z (Z+ and Z-) terminals for controlling the current transfer gain parameter k. The gain parameter k shows a variation from 1 to $(2^n - 1)$, where n is the number of transistor arrays. The modified circuit of DVCC with the transistors arrays is as shown in Figure 5. The CSN consists of n transistor pairs, the aspect ratios of whose PMOS and NMOS transistors respectively are given by:

$$\left(\frac{W}{L}\right)_i = 2^i \left(\frac{W}{L}\right)_9 \quad (9)$$

$$\left(\frac{W}{L}\right)_i = 2^i \left(\frac{W}{L}\right)_{12} \quad (10)$$

Furthermore, the current at the Z terminal which is assumed to be flowing out of the DC-DVCC, can be expressed by:

$$I_z = \sum_{i=0}^{n-1} d_i 2^i \left(I_9 - I_{12}\right) \quad (11)$$

Therefore, the proposed DC-DVCC provides a current transfer gain, k equal to:

$$k = \frac{I_z}{I_X} = \frac{\sum_{i=0}^{n-1} d_i 2^i \left(I_9 - I_{12}\right)}{\left(I_9 - I_{12}\right)} = \sum_{i=0}^{n-1} d_i 2^i \quad (12)$$

Where d_i are the bits applied to the i-th branch in the CSN. Now the current flow in a particular branch is enabled or disabled depending upon whether d_i is a logic 1 or logic 0 [16].

4. Comparative Study of Variation in Bandpass Filter Resonant Frequency

In this section the discussion is restricted to the variation in resonant frequency of Band Pass filter only. The circuit shown in Figure 3 was modified by replacing a DVCC block with a DC-DVCC block, one by one so that change in relationship between the resonant frequency and control word can be observed. Each block is assigned an individual gain α, β and γ respectively. The analysis is done and the following expression was obtained for the band pass response.

$$\frac{I_{BP}}{I_{IN}} = -\frac{s\frac{\alpha\beta R_1}{R_2R_3C_1}}{s^2 + s\alpha\left(\frac{1}{R_2C_1}\right) + \frac{\alpha\beta\gamma R_1}{R_2R_3R_4C_1C_2}} \quad (13)$$

The resonant frequency is now defined as

$$= \sqrt{\frac{\alpha\beta\gamma R_1}{R_2R_3R_4C_1C_2}} \quad (14)$$

As could be clearly seen from (14) the resonant frequency of the Bandpass filter can be controlled by changing the values of the gain parameters α, β and γ. This variation will not require any change in the values of the passive components.

In the analysis that follows it is assumed that if the DVCC is replaced by DC-DVCC the gain parameter for respective block takes the value k, however if the DVCC is retained, the gain parameter attains value equal to 1.

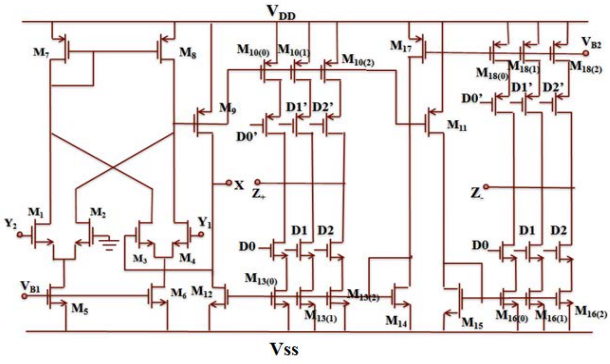

Figure 5. CMOS realization of the DC- DVCC having gain k

Replacing the first block (corresponding to α) by DC-DVCC, therefore for this configuration we have α= k and β=γ= 1, hence the equation for the band-pass response and the expression for the resonant frequency are respectively given by:

$$\frac{I_{BP}}{I_{IN}} = -\frac{s\frac{kR_1}{R_2R_3C_1}}{s^2 + sk\left(\frac{1}{R_2C_1}\right) + \frac{kR_1}{R_2R_3R_4C_1C_2}} \quad (15)$$

$$= \sqrt{\frac{kR_1}{R_2R_3R_4C_1C_2}} \quad (16)$$

The configuration is illustrated in Figure 6.

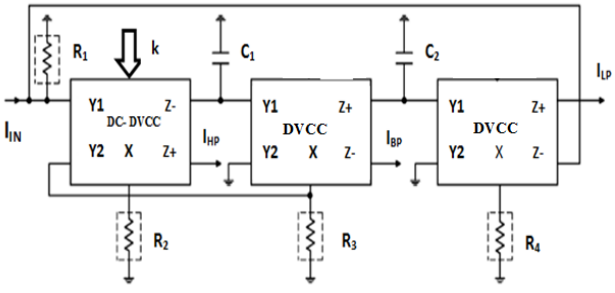

Figure 6. Configuration for α= k and β=γ= 1

From (16) it is evident that the resonant frequency varies with the control word k, in a square root fashion. The configuration shown in Figure 6 is simulated using PSPICE and the Bandpass reses obtained for the control word ([0 0 1] and [1 1 1]) are shown in Figure 7 (a) and Figure 7 (b).

Figure 7(a). Simulated magnitude response (in dB) for band pass filter with control word [$d_2\,d_1\,d_0$ = 0 0 1] selected for circuit of Figure 6

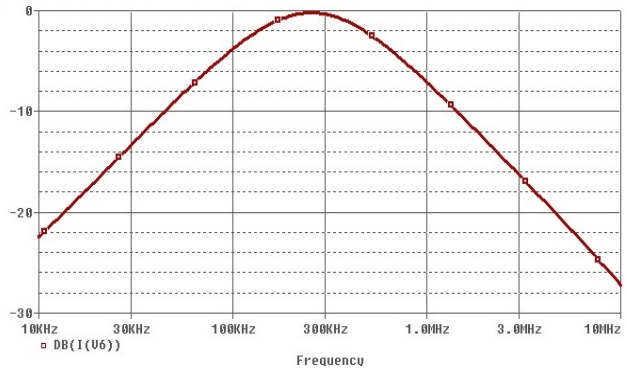

Figure 7(b). Simulated magnitude response (in dB) for band pass filter with control word [$d_2\,d_1\,d_0$ = 1 1 1] selected for circuit of Figure 6.

The simulations show a gradual increase in the resonant frequency when the control word is increased, the observations are recorded in Table II.

Now when the second block is replaced the value of the gain parameters changes to α= β=k and γ= 1 hence the equation for the band-pass response and the expression for the resonant frequency are respectively given by:

$$\frac{I_{BP}}{I_{IN}} = -\frac{s\dfrac{k^2R_1}{R_2R_3C_1}}{s^2 + sk\left(\dfrac{1}{R_2C_1}\right) + \dfrac{k^2R_1}{R_2R_3R_4C_1C_2}} \tag{17}$$

$$= k\sqrt{\frac{R_1}{R_2R_3R_4C_1C_2}} \tag{18}$$

The configuration is illustrated in Figure 8

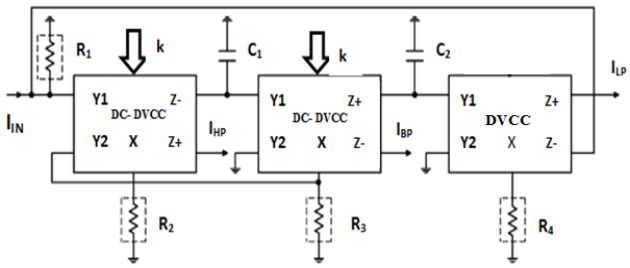

Figure 8. Configuration for α= k and β=γ= k

From (18) it is evident that the resonant frequency varies with the control word k, in a linear fashion. The configuration shown in Figure 8 is simulated using PSPICE and the Bandpass reses obtained for the control word ([0 0 1] and [1 1 1]) are shown in Figure 9 (a) and Figure 9 (b).

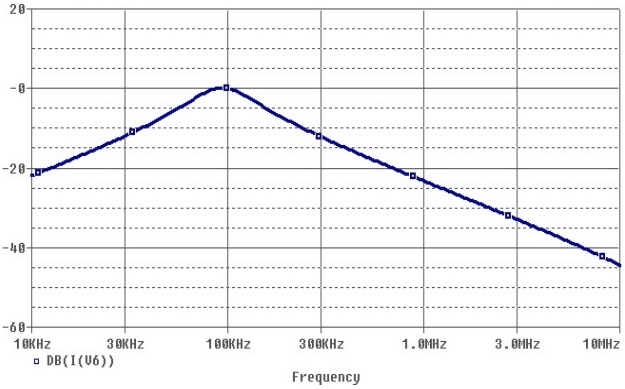

Figure 9(a). Simulated magnitude response (in dB) for band pass filter with control word [$d_2\,d_1\,d_0$ = 0 0 1] selected for circuit of Figure 8

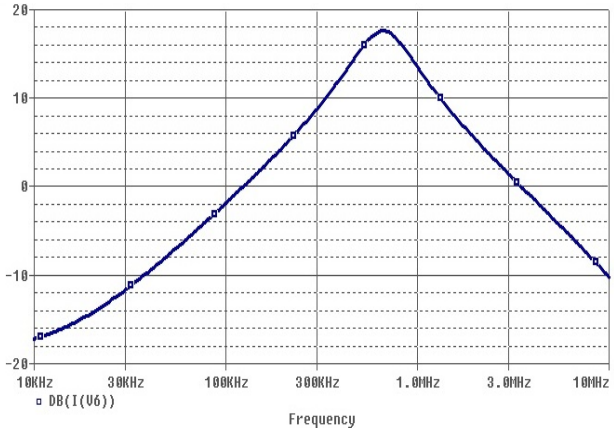

Figure 9(b). Simulated magnitude response (in dB) for band pass filter with control word [$d_2\,d_1\,d_0$ = 11 1] selected for circuit of Figure 6

The simulations show an increase in the resonant frequency when the control word is increased, the observations are recorded in Table 2.

When the third block is replaced the value of the gain parameters changes to α= β=γ=k hence the equation for the band-pass response and the expression for the resonant frequency are respectively given by:

$$\frac{I_{BP}}{I_{IN}} = -\frac{s\dfrac{k^2R_1}{R_2R_3C_1}}{s^2 + sk\left(\dfrac{1}{R_2C_1}\right) + \dfrac{k^3R_1}{R_2R_3R_4C_1C_2}} \tag{19}$$

$$= k^{3/2}\sqrt{\frac{R_1}{R_2R_3R_4C_1C_2}} \tag{20}$$

The configuration is illustrated in Figure 10

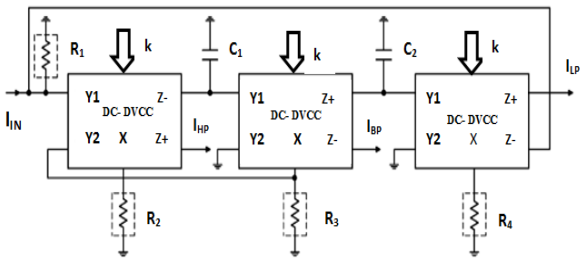

Figure 10. Configuration for α= β=γ= k

From (20) it is evident that the resonant frequency varies with the control word k, in a $k^{3/2}$fashion. The

configuration shown in Figure 10 is simulated using PSPICE and the Bandpass reses obtained for the control word ([0 0 1] and [1 1 1]) are shown in Figure 11 (a) and Figure 11 (b).

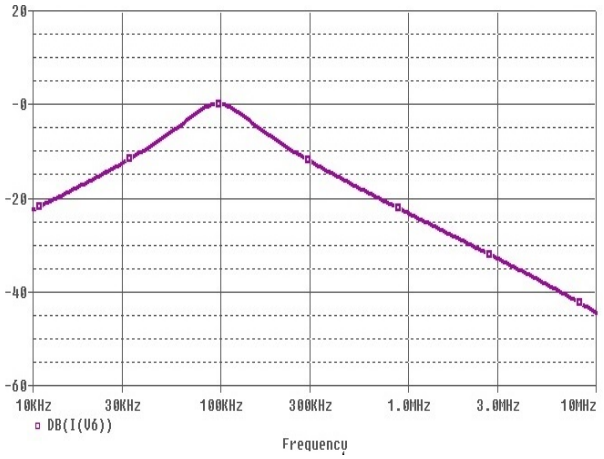

Figure 11(a). Simulated magnitude response (in dB) for band pass filter with control word [$d_2\, d_1\, d_0$ = 0 0 1] selected for circuit of Figure 10

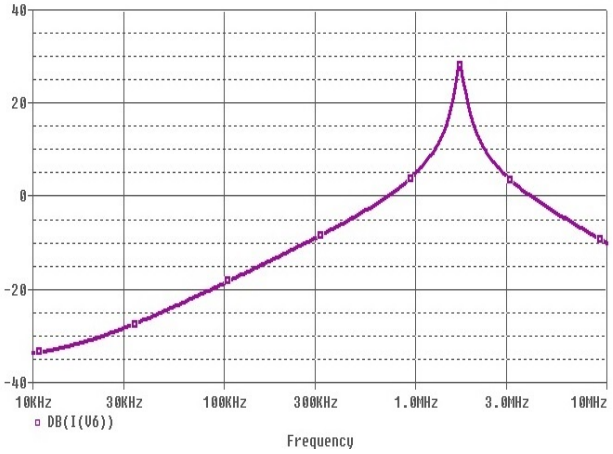

Figure 11(b). Simulated magnitude response (in dB) for band pass filter with control word [$d_2\, d_1\, d_0$ = 1 1 0] selected for circuit of Figure 10

The simulations show an increase in the resonant frequency when the control word is increased, the observations are recorded in Table 2.

The circuit presented in [14] for a particular design worked only for a single frequency but using the modification suggested in this paper the utility of the circuit is increased.

Now the circuit when selected for a particular variation and designed for a particular set of values of resistances and capacitances can work for seven different frequencies.

Table 2. Variation in resonant frequency of bandpass responses with the control word

Control word, k	Resonant frequency of BPF of Circuit of Figure 10 (kHz) $(\omega \propto k^{3/2})$	Resonant frequency of BPF of Circuit of Figure 8 (kHz) $(\omega \propto k)$	Resonant frequency of BPF of Circuit of Figure 6 (kHz) $(\omega \propto \sqrt{k})$
1	97.79	93.51	95.63
2	270.40	187.00	135.23
3	491.75	282.78	166.29
4	759.70	380.27	191.23
5	1045.13	475.54	213.84
6	1376.03	568.66	235.16
7	1689.10	661.28	257.16

Figure 12, Figure 13 and Figure 14 are the plots showing variation in resonant frequency of the Bandpass filter configurations shown in Figure 6, Figure 8, Figure 10.

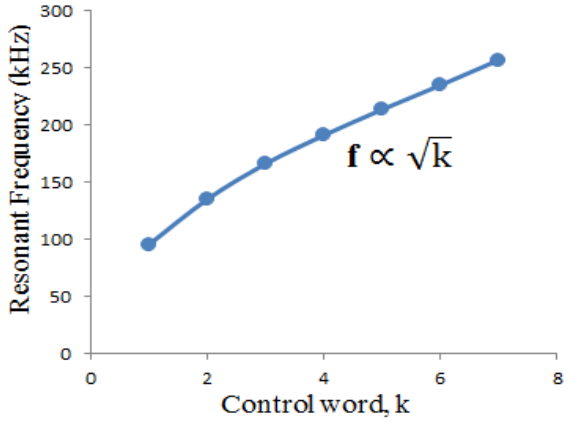

Figure 12. Variation in resonant frequency of BPF with digital control word for circuit of Figure 6

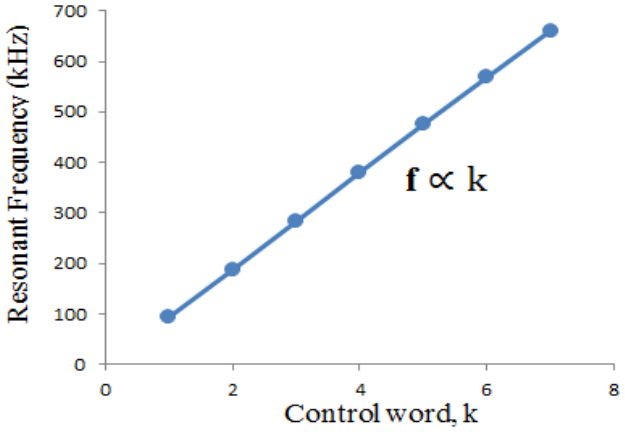

Figure 13. Variation in resonant frequency of BPF with digital control word for circuit of Figure 8

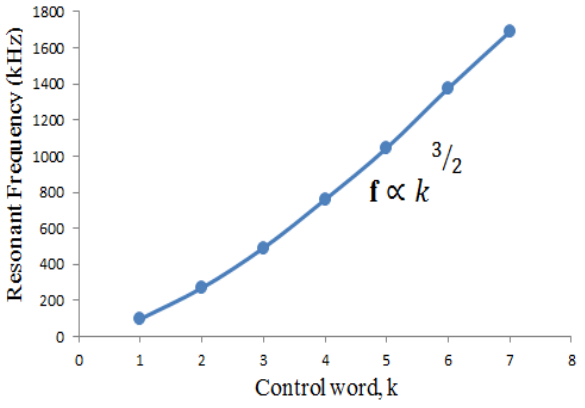

Figure 14. Variation in resonant frequency of BPF with digital control word for circuit of Figure 10

The plots for the variation in resonant frequency obtained by simulation support the theoretical analysis. For the circuit in Figure 6 we have obtained a square root variation then linear variation is observed for the circuit of Figure 8 finally a variation directly proportional to $k^{3/2}$ is observed for circuit of Figure 10.

5. Conclusion

In this paper, a digitally programmable current mode K.H.N. biquad filter based on three DVCCs was presented. Digital control has been achieved with the introduction of CSNs and variation of 3-bit digital control word (k). Now this circuit can be tuned for seven different frequencies for a particular design and variation. This multi frequency tenability within the same design is the contribution for this circuit The circuit was configured in three different ways to provide different relation between resonant frequency of the Bandpass filter and the digital control word (k). The variations obtained were dependent upon the number of DC-DVCCs used. When a single DVCC was replaced with a DC-DVCC square root relation between resonant frequency and k was obtained, this variation became linear on replacement of second DVCC block and when the final block was replaced the resonant frequency became directly proportional to $k^{3/2}$. The observations support the fact that the resonant frequency of Bandpass filter is directly proportional to $k^{a/2}$, where 'a' is the number of DVCC replaced with DC-DVCC. Hence we obtained a circuit whose variation (relationship) of resonant frequency can be controlled. PSPICE simulations were carried out to verify the working of the digitally controlled K.H.N. Biquad Filter.

References

[1] H. O. Elwan, A. M. Soliman. "A novel CMOS current conveyor realization with an electronically tunable current mode filter suitable for VLSI." *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions*, vol. 43, issue. 9, pp. 663-670, Sep. 1996.

[2] C.M. Chang, M.J. Lee. "Voltage-mode multifunction filter with single input and three outputs using two compound current conveyors." *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions*, vol. 46, issue. 11, pp. 1364-1365, Nov. 1999.

[3] O. Cicekoglu. "Current-mode biquad with a minimum number of passive elements." *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions*, vol. 48, issue. 2, pp. 221-222, Feb. 2001.

[4] H. Y. Wang, C. T. Lee. "Versatile insensitive current-mode universal biquad implementation using current conveyors." *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions*, vol. 48, issue. 4, pp. 409-413, Apr. 2001.

[5] A.S. Sedra, K.C. Smith. "A second generation current conveyor and its applications". *IEEE Transactions on circuit theory*, vol. 17, pp.132-134, Feb. 1970.

[6] W. Chiu, S. I. Liu, H. W. Tsao, J. J. Chen. "CMOS differential difference current conveyors and their applications." *IEE Proceedings-Circuits, Devices and Systems*, vol. 143, issue. 2, pp. 91-96, Apr. 1996.

[7] H.O. Elwan, A. M. Soliman. "Novel CMOS differential voltage current conveyor and its applications." *IEE Proceedings-Circuits, Devices and Systems*, vol. 144, issue. 3, pp. 195-200, Jun. 1997.

[8] T. Dostal, D. Biolek, K. Vrba. "Adjoint voltage-current mode transformation for circuits based on modern current conveyors." *Devices, Circuits and Systems, Proceedings of the Fourth IEEE International Caracas Conference*, 2002, pp. T034-1.

[9] B. Wilson, "Recent developments in current conveyors and current-mode circuits." *Circuits, Devices and Systems, IEE Proceedings G*, vol. 137, issue. 2, pp. 63-77, Apr.1990.

[10] H. Hakan Kuntman. "New Advances and Possibilities in Active Circuit Design." in *Proc. 10th International Conference on Development and Application Systems*, 2010, pp. 9-18.

[11] H. P. Chen and S. S. Shen. "A versatile universal capacitor-grounded voltage-mode filter using DVCCs." *ETRI journal*, vol. 29, issue. 4, pp. 470-476, Aug. 2007.

[12] H. P. Chen. "Tunable versatile current-mode universal filter based on plus-type DVCCs." *AEU-International Journal of Electronics and Communications*, vol. 66, issue. 4, pp. 332-339, 2012.

[13] I. A. Khan and A. M. Nahhas. "Reconfigurable Voltage Mode First Order Multifunctional Filter using Single Low Voltage Digitally Controlled CMOS CCII." *International Journal of Computer Applications*, vol. 45, issue. 5, pp. 37-40, May. 2012.

[14] M.A. Ibrahim, S. Minaei, H. Kuntman. "A 22.5 MHz current-mode KHN biquad using differential voltage current conveyor and grounded passive elements." *AEU-International Journal of Electronics and Communications*, vol. 59, issue. 5, pp. 311-318, 2005.

[15] W. Tangsrirat, O. Chaannumsin. "Voltage -mode multifunctional biquadratic filter using single DVCC and minimum number of passive elements". *Indian Journal of Pure and Applied Physics*, vol. 49, pp.703-707, Oct. 2011.

[16] S. A. Mahmoud, M.A. Hashiesh. and A.M. Soliman. "Low-voltage digitally controlled fully differential current conveyor." *Circuits and Systems I: Regular Papers, IEEE Transactions*, vol. 52, issue. 10, pp. 2055-2064, Oct. 2005.