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# Synthetic Floating Inductors realized with only two Current Feedback Op-amps 

D. R. Bhaskar ${ }^{1}$, R. Senani ${ }^{2, *}$<br>${ }^{1}$ Department of Electronics and Communication Engineering, Jamia Millia Islamia, New Delhi, India<br>${ }^{2}$ Devision of Electronics and Communication Engineering, Netaji Subhas Institute of Technology, New Delhi, India<br>*Corresponding author: senani@ieee.org

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#### Abstract

Two floating inductance (FI) circuits are presented which employ a canonical number of passive components (namely, only two resistors and a capacitor) as well as canonical number of active elements (only two CFOAs) and realize single-resistance-tunable inductance value, without requiring any component-matching or cancellation constraints. The workability of the proposed circuits and their applications has been confirmed by hardware implementation and SPICE simulations based on AD844-type CFOAs.


Keywords: inductance simulation, current feedback op-amps, floating inductance simulation, analog circuits
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## 1. Introduction

The simulation of grounded inductance (GI) and floating inductance (FI) has continued to remain an important and popular area of analog circuits research due to their applications in linear (active filters and oscillators) and nonlinear (such as chaotic oscillators) circuit designs.

Although inductance simulation circuits using a large number of active building blocks have been reported in the recent literature, those using current conveyors (CCs) and current feedback operational amplifiers (CFOAs) have found prominent place particularly due to the commercial availability of a CFOA with externally accessible z-pin such as AD844 which can be used to realize both CCbased as well as CFOA-based inductance simulators practically.

It was demonstrated in [1,2,3,4], for the first time, that using CCII- as building blocks, it becomes possible to realize FI simulation circuits using only three passive components without requiring any component-matching condition(s)- a feat which was impossible to be achieved by op-amp-RC circuits prevalent in those days. Later, when CFOA AD844 came into existence, it was demonstrated by Fabre in [5] that a grounded loss-less inductance can be simulated using two CFOAs and only three passive components (namely, two resistors and a capacitor) without any component-matching condition. In [6], it was shown that loss-less FI can be realized with only three CFOAs, three passive components and still not requiring any matching conditions. The latter works [7][13] have demonstrated a variety of grounded impedance simulation circuits all employing only a single CFOA with the exception of [13] in which case two CFOAs are
utilized and [14] wherein three CFOAs are employed to realize a grounded-capacitor (GC) based GI ${ }^{1}$.

Among the CFOA-based loss-less FI circuits, those in [6] and [15] (derived from the biquad of [16]) require three CFOAs, two resistors and a GC as preferred for integrated circuit implementation [17,18]. The circuits of [19,20,21] employ as many as four CFOAs although they can realize a larger variety of floating Impedances such as floating FDNR and floating FDNC also besides a FI. On the other hand, the circuit of [22] although employs a canonical number of passive components to realize lossless FI but requires four current conveyors. Recently, the present authors reported a two CFOA-based circuit [23] which simulates a lossy/lossless floating inductance (FI) employing three resistors and two capacitors. However, the circuit of [23] uses a non-canonical number of resistors (three rather than two) and capacitors (two instead of one) and moreover, needs one cancellation constraint for realizing a lossless FI.

The purpose of this communication is to discuss two lossy $\mathrm{FI}^{2}$ circuits which, like the circuit of [23], require only two CFOAs but by contrast, provide the following features not available in the earlier circuit of [23], namely: (i) employment of only a single capacitor along with a minimum number of (only two) resistors (ii) no requirement of any realization condition/cancellation constraint to realize the intended type of impedances and

[^0](iii) realizability of single-resistance-tunability of the inductance value. The workability of the described circuits has been confirmed by hardware implementation results and SPICE simulations based on AD844 type CFOAs.

## 2. Synthetic FI Circuits Realized with only Two CFOAs

Consider now the circuits shown in Figure 1. Assuming CFOAs to be characterized by $i_{y}=0, v_{x}=v_{y}, i_{z}=i_{x}$ and $v_{w}$ $=\mathrm{v}_{\mathrm{z}}$, a straight forward analysis of the proposed circuits reveals their Y-matrices to be given by:

$$
[\mathrm{Y}]=\left[\frac{1}{R_{1}+s C_{0} R_{1} R_{2}}\right]\left[\begin{array}{cc}
1 & -1  \tag{1}\\
-1 & 1
\end{array}\right]
$$

for the circuit of Figure 1(a) and

$$
[Y]=\left[\frac{1}{R_{1}}+\frac{1}{s C_{0} R_{1} R_{2}}\right]\left[\begin{array}{cc}
1 & -1  \tag{2}\\
-1 & 1
\end{array}\right]
$$

for the circuit of Figure 1(b).
Thus, the circuit of Figure 1(a) simulates a floating series-RL impedance with equivalent resistance $R_{\text {eq }}=R_{1}$ and equivalent inductance $\mathrm{L}_{\text {eq }}=\mathrm{C}_{0} \mathrm{R}_{1} \mathrm{R}_{2}$, while the circuit of Figure 1(b) simulates a parallel-RL admittance with $R_{e q}=R_{1}$ and $L_{e q}=C_{0} R_{1} R_{2}$. In both the circuits, the value of $\mathrm{L}_{\mathrm{eq}}$ is controllable independently of the associated resistive part by a single variable resistance $\mathrm{R}_{2}$.


Figure 1. The canonic floating inductance simulators (a) series-RL FI simulator (b) parallel-RL FI simulator

From equations (1) and (2), it can be readily deduced that the various sensitivity coefficients of the realized equivalent inductance and resistance with respect to passive elements would be in range of

$$
\begin{equation*}
0 \leq\left|S_{x_{i}}^{F}\right| \leq 1 \tag{3}
\end{equation*}
$$

where $F$ represents $L_{\text {eq }}$ or $R_{\text {eq }}$ and $x_{i}$ represents any of $R_{1}$, $R_{2}$ and $C_{0}$ and the circuits, thus, enjoy low sensitivity properties.

## 3. The Effect of Non-ideal Parameters of the CFOAs

Considering the various non-ideal parasitic impedances of the CFOAs, namely, the finite input impedance looking into terminal- X as $\mathrm{R}_{\mathrm{X}}$, the output impedance looking into terminal-Z $\left(Z_{p}\right)$ consisting of a parasitic resistance $R_{P}$ in parallel with a parasitic capacitance $\mathrm{C}_{\mathrm{p}}$ and the input impedance looking into Y-terminal $\left(\mathrm{Z}_{\mathrm{Y}}\right)$ consisting of a parasitic resistance $R_{Y}$ in parallel with a parasitic capacitance $\mathrm{C}_{\mathrm{Y}}$, the non-ideal Y-parameters of the two circuits are found to be:
For the circuit of Figure 1(a)

$$
\begin{gather*}
Y_{11}^{\prime}=\frac{1}{D_{1}(s)}=-Y_{21}^{\prime}  \tag{4}\\
Y_{12}^{\prime}=\frac{-\left(1+\frac{R_{2}}{Z_{Y}}\right)}{D_{1}(s)}=-Y_{22}^{\prime}  \tag{5}\\
D_{1}(s)=\left(R_{1}+2 R_{X}\right)\left(1+s C_{0} R_{2}+\frac{R_{2}}{Z_{Y}}\right) \tag{6}
\end{gather*}
$$

For the circuit of Figure 1(b)

$$
\begin{equation*}
Y_{11}^{\prime}=\frac{N_{1}(s)-N_{2}(s)}{D_{2}(s)} \tag{7}
\end{equation*}
$$

where

$$
\begin{equation*}
N_{1}(s)=\frac{s C_{0}}{R_{1}}+\frac{1}{R_{2}}\left(\frac{1}{R_{1}}+\frac{1}{Z_{p}}\right) \tag{8}
\end{equation*}
$$

and

$$
\begin{gather*}
N_{2}(s)=\left(\frac{R_{X}}{Z_{P}}\right)\left(s C_{0}+\frac{1}{R_{2}}+\frac{1}{Z_{Y}}\right)\left(\frac{1}{Z_{P}}+\frac{2}{R_{1}}\right)  \tag{9}\\
Y_{12}^{\prime}=\frac{\left(\frac{1}{R_{1}}+\frac{1}{Z_{P}}\right)\left(s C_{0}+\frac{1}{R_{2}}+\frac{1}{Z_{Y}}\right)}{D_{2}(s)}  \tag{10}\\
Y_{21}^{\prime}=\frac{\left\{\frac{1}{R_{1} R_{2}}+s C_{0}\left(\frac{1}{R_{1}}+\frac{1}{Z_{P}}\right)\right\}}{D_{2}(s)}  \tag{11}\\
Y_{22}^{\prime}=\frac{\left(\frac{1}{R_{1}}-\frac{R_{X}}{Z_{P}^{2}}-\frac{2 R_{X}}{R_{1} Z_{P}}\right)\left(s C_{0}+\frac{1}{R_{2}}+\frac{1}{Z_{Y}}\right)}{D_{2}(s)} \tag{12}
\end{gather*}
$$

where

$$
\begin{align*}
& D_{2}(s)=s C_{0}\left(1+\frac{R_{X}}{R_{1}}\right)+R_{X}\left\{\left(\frac{1}{Z_{P} R_{2}}+\frac{1}{R_{1} R_{2}}\right)\right.  \tag{13}\\
& \left.+\left(s C_{0}+\frac{1}{R_{2}}+\frac{1}{Z_{Y}}\right)\left(\frac{1}{R_{1}}-\frac{R_{X}}{Z_{P}^{2}}-\frac{2 R_{X}}{R_{1} Z_{P}}\right)\right\}
\end{align*}
$$

Note that if we take $Z_{P} \rightarrow \infty, Z_{Y} \rightarrow \infty$, and $R_{X} \rightarrow \infty$, the non-ideal Y-parameters approach their ideal values as given in equations (1) and (2). From the non-ideal Yparameters, it is clear that like all other FI circuits, the performance of both the circuits will depart from its ideal intended one, at high frequencies.

A comparison of the various features of the proposed circuits with CFOA-based and CCII-based (realizable with CFOAs) loss-less/lossy FI circuits known earlier has been carried out in Table 1. In making this table, it is taken into account that a CCII+ is realizable with one CFOA whereas a CCII- can be realized with two CFOAs).

Table 1. Comparison with the Earlier Known Circuits

| Ref. | Number and type of blocks used | Canonic in number of Passive elements? | Number of CFOAs used | Free from matching? | Can $\mathrm{L}_{\text {eq }}$ be tuned? |
| :---: | :---: | :---: | :---: | :---: | :---: |
| [19] | 4; CFOA | No | 4 | Yes | Yes |
| [20] | 4; CFOA | No | 4 | Yes | Yes |
| [4] | 2; CCII- | No | 4 | Yes | Yes |
| [15] | 3; CFOA | Yes | 3 | Yes | Yes |
| [6] | 3; CFOA | Yes | 3 | Yes | Yes |
| [1] | 1; CCII- | Yes | 2 | Yes | No |
| [2] | 3/2; CCII- | Yes | 4 | Yes | Yes |
| [23] | 2; CFOA | No | 2 | No | No |
| This work | 2; CFOA | Yes | 2 | Yes | Yes |

From Table 1, it is clear that the circuits presented in this paper are the only ones which possess the following properties simultaneously, namely, (i) employment of a canonical number of passive components (ii) employing only two CFOAs (iii) complete absence of any component-matching requirements and (iv) single-resistor-tunability of the realized FIs.

## 4.Experimental and Simulation Results

The validity of the proposed FI simulators has been verified by implementing them with commercially available AD844-type CFOAs and 5\% tolerance RC elements, as well as by SPICE simulations based upon a macromodel of AD844.


Figure 2. Frequency response of the BPF realized from the proposed FI of Fig. 1 (a)

The workability of the simulated FI configuration of Figure 1(a) has been verified by employing it in the realization of a tunable band pass filter (BPF), by connecting a capacitor $\mathrm{C}_{1}$ in series with its port-1 (or port 2) of the simulated inductor, with a resistor $R_{L}$ connected at its port 2 (or port 1 ) and then taking the output as the voltage across $\mathrm{R}_{\mathrm{L}}$. The component values chosen were: (i) Set-I: $\mathrm{R}_{1}=1 \mathrm{k} \Omega=\mathrm{R}_{2}=\mathrm{R}_{\mathrm{L}}, \mathrm{C}_{1}=1 \mathrm{nF}=\mathrm{C}_{0}$ and (ii) Set-II: $\mathrm{R}_{1}=\mathrm{R}_{\mathrm{L}}=1 \mathrm{k} \Omega, \mathrm{R}_{2}=4.7 \mathrm{k} \Omega, \mathrm{C}_{1}=1 \mathrm{nF}=\mathrm{C}_{0}$ chosen to provide theoretical values of $\mathrm{f}_{0}$ as 159 kHz and 73.34 kHz
respectively. The experimental results of these designs have been shown in Figure 2 wherein the experimental values of $\mathrm{f}_{0}$ have been found to be 159 kHz and 74 kHz respectively. The experimental results of Figure 2, thus, confirm the workability as well as the tunability of the inductance value (and hence, $f_{0}$ ) with $R_{2}$.

The workability of the parallel- RL FI of Figure 1(b) has been confirmed by using it in the design of a $4^{\text {th }}$ order Butterworth filter based upon the normalized passive RLC prototype of Figure 3(a) and using transformation T-2 ${ }^{3}$ from [25,26]. This transformation scales all the impedances of the RLC prototype of Figure 3(a) by a frequency-dependent scaling factor $\mathrm{F}(\mathrm{s})=1 /(1+\mathrm{s})$ which transforms a resistor into a parallel RC, an inductor into a parallel RL and a capacitor into a parallel combination of a capacitor and a FDNR (frequency-dependent-negativeresistance; an element having impedance of type $\mathrm{Z}(\mathrm{s}$ ) $=1 / D s^{2}$ ), as shown in Figure 3(b). Note that in the transformed circuit of Figure 3(b), the floating parallel RL simulator of Figure 1(b) can be employed directly in place of both the parallel-RL branches. Furthermore, the two shunt CD-branches can also be simulated from the RC: CR transformed version of the circuit of Figure 1(b) with anyone of its two ports grounded. However, such a circuit would require two CFOAs for each grounded shunt parallel CD branch and would not be economical. Hence, to reduce the total component count, instead of using the suggested two- CFOA-based circuit, we have used a simpler one-CFOA-based circuit shown in Figure 3(c) to simulate both the shunt-CD branches encountered in the transformed prototype of Figure 3(b). The final circuit, thus, obtained has been shown in Figure 3 (d).

This circuit enables direct incorporation of the lossy FI of Figure 1(b) and grounded CD branch realized with a single CFOA circuit of Figure 3(c) into the design where the component values, as shown, have been obtained for a de-normalized cut-off frequency of $f_{0}=100 \mathrm{kHz}$.

The SPICE simulations have revealed the cut-off frequency as 98 kHz which is quite close to the theoretical value of 100 kHz . The SPICE-generated frequency response of the circuit is shown in Figure 3(e). These simulation results, thus, confirm the workability of the FI circuit of Figure 1(b).

[^1]

Figure 3. Application and SPICE simulation results of the FI circuit of Figure 1(b): (a) Normalized 4th-order Butterworth Low Pass Filter; (b) Filter obtained by applying Senani’s transformation T-2 from [25,26] on the circuit of Figure 3(a); (c) An exemplary realization of a grounded parallel CD branch; (d) Final $4^{\text {th }}$ - order Butterworth active filter obtained by replacing various RL and CD immittances of Figure 3(b) by the circuits of Figure 1(b) and Fig 3 (c); (e) SPICE generated Frequency response of the 4th-order Butterworth Low Pass Filter of Figure 3(d)

## 5. Discussions

Note that, in case of the BPF responses of Figure 2 while SPICE simulations take all the passive component values to be exact, in hardware implementation, RC components used were having 5\% tolerances (hence, were not exact). As a consequence, the deviation of the practical responses from that exhibited by SPICE simulations is attributed to the passive component tolerances.

Further, it must be mentioned that the circuit of Figure 3(d) should not be taken as the recommended best method to design a $4^{\text {th }}$ order Butterworth filter using CFOAs. This particular method has been applied here only as a vehicle to demonstrate the use of the FI of Figure 1(b) and to check its workability in higher order filter designs.

## 6. Concluding Remarks

Two canonic synthetic floating inductors have been discussed which, like the recently proposed FI of [23], use only two CFOAs, however, in contrast to the earlier
circuit of [23], which requires two matched capacitors, three resistors (two of which are also required to be identical) and a cancellation constraint (for realizing a lossless FI), the discussed circuits provide the following advantageous features which are not available simultaneously either in the FI circuit of [28] or any other CC/CFOA based FIs known earlier: (i) use of a canonical number of passive components namely, only a single capacitor and two resistors (ii) employment of only two CFOAs for realizing an FI (iii) realization of the intended type of FIs without requiring any equality constraints or cancellation conditions, and (iv) the availability of single-resistance-tunability of the realized equivalent inductance value in both the cases.

The workability of the discussed FI circuits has been confirmed by experimental results and SPICE simulations based upon AD844-type CFOAs.

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[^0]:    ${ }^{1}$ Although reference [24] shows that three passive elements and a single modified CFOA are sufficient to realize a variety of grounded impedances but the so-called modified CFOA is, in fact, actively realized from a composite connection of a CCII + and a CCII- and therefore, would call for at least three CFOAs of the normal kind (one for CCII + and two for the CCII-).
    ${ }^{2}$ The circuit of Figure 1(a) was briefly presented in a conference [27] and before that, had been mentioned in [33], as an unpublished circuit. However, the circuit of Figure 1(b) is completely new.

[^1]:    ${ }^{3}$ For further details of the various transformations, see [25,26].

