

Research and Mitigation on EMI Noise for PV Converter

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Abstract Photovoltaic (PV) systems have been widely used for power generation and renewable energy. Conducted electromagnetic interference (EMI) noise have generated, which affect the performance of other device and the grid. In the paper, the measurement uncertainty of artificial mains network (AMN) has been analyzed. The conducted EMI noise mechanism and noise mitigation methods have been proposed, including transistor filter and well grounding design strategies. The simulation and experiment results show that the conducted EMI noise generated by a certain convert can be suppressed well and pass EN 55011 and EN 55022 standards, thus good realization and validation.

Keywords: Photovoltaic (PV) converter, electromagnetic interference (EMI), conducted EMI, noise reduction

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1. Introduction

For energy safety and renewable, photovoltaic systems have been widely used for power generation [1,2,3]. The direct current (DC) can be obtained from photo through solar cells. And the DC signals transfer to the alternating current (AC) signals by employing the photovoltaic converters. Due to the performance and operation of PV converters, much conducted EMI noises are generated based on switch mode transistors, control strategy, high frequency chips, parasitic inductance and capacitors and topology [4,5,6,7,8], as shown in Figure 1.

Firstly, the transistors T_{11} , T_{12} , T_{21} , T_{22} , T_{31} , T_{32} can generate very shape and steep current pulse di/dt through

switch-on and switch-off motion. And the pulse can couple into the output current and the grid. In general, the spectrum of the pulse is from several kilo hertz to several mega hertz. The time domain and frequency domain pulse wave is decided by the control strategy, including wave pattern, width, duty ratio and period.

Secondly, the conducted EMI noises above several mega hertz are produced by the high frequency chips, such as crystal oscillator, single chip microcomputer and signal acquisition chips.

Thirdly, the envelope of conducted EMI noises increases totally due to the grounding modes, including single point grounding, multi points grounding and hybrid grounding.

The last but not the least, the conducted EMI noises are generated by the topology of PV converter, such as circuit loop, parallel routing and so on.



Figure 1. The topology of PV converter

The conducted EMI noise mechanism are coupled and complicated due to the above four complicated reasons. Many researches have been proposed to study and solve the above problems. An AC EMI filter structure in the single-phase grid-interface converter was analyzed for low-voltage dc distribution system, which helps reduce the coupling between dc and ac-side, and thus simplifies the CM EMI filter design process [9]. A new inverter topology, buck-buck-boost (B3) inverter, which is derived from an H-bridge converter with additional switch legs, was designed to reduce the common mode noise due to its solid connection between the grounds of the input and output terminals [10]. A digital active EMI filter (DAEF), whose control technique is concurrently implemented with a digital controller of a grid-tied photovoltaic microinverter, was proposed to suppress common mode EMI noises. And the DAEF can achieve an equivalent or better performance in terms of EMI suppression and maintain stability within the operation bandwidth [11]. The performance of spread spectrum frequency modulation (SSFM) was evaluated to the EMI reduction of a real power converter that uses periodic pattern switching frequency modulation [12]. A new method is proposed to test the conducted and radiated electromagnetic interference (EMI) noise of photovoltaic invert based on analysis the internal structure and measuring principle of artificial mains network [13].

To solve the conducted EMI noise problems of PV converter, the measurement method, noise mechanism and noise mitigation approaches are analyzed and proposed in the paper.

2. Measurement Uncertainty Based on Artificial Mains Network

According to EN 55011 and EN 55022, conducted EMI noises should be determined by EMI receiver and artificial mains network (AMN), where both quasi peak detector and average detector are fixed on the EMI receiver. The setup of conducted EMI noise measurement for single phase was shown in Figure 2.



Figure 2. Conducted EMI noise measurement under EN 55011/ EN 55022 $\,$

Due to the parasitic capacitor and inductance of AMN, the test result of conducted EMI noise was uncertainty. According to CISPR 16, the topology structure is shown in Figure 3(a), where C_1 is 1µF, C_2 is 0.1µF, R_1 is 50 Ω , R_2 is 1k Ω and L_1 is 50µH. Concerned on the parasitic parameters of the above capacitors, inductances and resistances, the equivalent HF circuit was shown in Figure 3(b), where L_{esc1} and L_{esc2} are the parasitic inductance of C_1 and C_2 , respectively. C_{es11} is the parasitic capacitor of L_1 . L_{es} and R_{es} are the parasitic inductance and resistance of the interface adapter.



(a) Topology structure of AMN based on CISPR 16



(b) The equivalent high frequency circuit of AMN

Figure 3. The topology and parasitic parameters of AMN

As shown in Figure 3, any parasitic parameters can be ignored due to the design and manufacturing technique of AMN, but the parasitic inductance of the interface adapter L_{es} should be concerned for the different interfaces and converters.

To determine the impedance under PV converter side of AMN, L_{es} was considered as 10nH and 100nH, respectively, and the other parasitic parameters can be neglected due to the measurement circuit, as shown in Figure 4. The simulation results show that with the L_{es} and measurement frequency increasing, the impedance under SMPS side was increasing greatly.

Therefore, the proper AMN and the interface adapters should be designed and employed to determine the conducted EMI noise and decrease the uncertainty of the measurement.



Figure 4. The impedance under PV converter side of AMN concerned on the parasitic parameters

3. Noise Mechanism Identification

According to the different noise transmission paths, the conducted EMI noises can be considered as common mode (CM) noise and differential mode (DM) noises, where the CM noise is between live/neutral and ground lines, and the DM noise is between live and neutral lines.

$$U_{CM} = \frac{U_L + U_N}{2} \quad U_{DM} = \frac{U_L - U_N}{2}$$
(1)

where, U_{CM} and U_{DM} represent CM and DM noises, U_L and U_N denote live and neutral noises, respectively.

To reach the Eq(1) algorithm, four style of noise separation networks (NSN) were designed by Paul, See, Mardiguian and Guo based on high frequency transformer or power combiner/divider. To improve its characteristic and performance, a novel topology of NSN has been proposed, as shown in Figure 5. The voltage at the primary side of the high frequency transformer is the sum of the U_L and U_N . And the voltage at the secondary side of the high frequency transformer is the difference between U_L and U_N , which is consistent with the formula (1). Moreover, the CM choke at the secondary side can be mitigate the CM current, which will improve the NSN performance. The NSN can be placed between AMN and EMI receiver to extract the CM and DM noise.

To compare with the proposed NSN, Paul NSN, See NSN, Mardiguian NSN and GUO NSN, the performance characteristic of the NSN should be measured. By

employing the vector network analyzer (VNA), the CM insertion loss (CMIL), DM insertion loss (DMIL), CM rejection ratio (CMRR) and DM rejection ratio (DMRR) have been obtained, as shown in Table 1. The CMIL, DMIL, CMRR and DMRR is better than other type NSNs.



Figure 5. A novel topology of NSN

Table 1. Characteristic and performance of the different NSNs

| Туре | CMIL | DMIL | CMRR | DMRR |
|------------|--------|--------|---------|--------|
| | @30MHz | @30MHz | @30MHz | @30MHz |
| Paul | -4 dB | -15 dB | -3 dB | -25 dB |
| See | -5 dB | -16 dB | -5.5 dB | -20 dB |
| Mardiguian | -2 dB | -24 dB | -1.5 dB | -27 dB |
| Guo | -2 dB | -24 dB | -1.3 dB | -30 dB |
| Novel | -2 dB | -24 dB | -1 dB | -34 dB |



Figure 6. The topology and parasitic parameters of AMN

The novel NSN has been used to extract the CM and DM noises generated from switched reluctance motor (SRM), whose rated voltage and power are 220V and 3kW, respectively. But the loads of the SRM are 1kW and 2.5kW. As shown in Figure 6, the experiment results demonstrate the novel NSN has good performance and validation.

4. Noise Reduction Scheme

The different noise reduction methods should be used to solve the CM and DM noises, such as CM and DM filters. Two situations have been analyzed as follows.

4.1. Transistor Filtering

The switch velocity and frequency are controlled under different strategies, while some high frequency noises from 9kHz to 30MHz can be coupled into the power line. To reduce the high frequency noises, the filter capacitor can be shunt between the collector and emitting electrodes the bipolar junction transistor (BJT), similarly, the filter capacitor can also be shunt between the source and drain electrodes of the metal oxide semiconductor field effect transistor (MOSFET).

Moreover, the value of the capacitor should be smaller than 0.1μ F not only for the noise mitigation but also for the safety regulations & design.

4.2. Well Grounding

No well grounding can generate much more conducted noises, especially the CM noises, whose equivalent transmission circuit is shown in Figure 7(a). The measurement result of the load can be derived from Eq.(2).

$$U_{load} = \frac{Z_{load}}{Z_{CM} + Z_{load}} U_{CM} \tag{2}$$

where, U_{CM} denotes the equivalent voltage source of CM noise, U_{load} represents the measurement result of the load, Z_{CM} and Z_{load} signify the equivalent impedance of the CM noise and the load. As shown in Figure 7(b), when the load was floating ground, the capacitor between floating ground and ground should be considered. And the measurement result of the equivalent load can be derived from Eq.(3).

$$U_{load}' = \frac{Z_{load} + \frac{1}{j\omega C}}{Z_{CM} + Z_{load} + \frac{1}{j\omega C}} U_{CM}$$
(3)

where, U'_{load} represents the measurement result of the equivalent load, C denotes the parasitic capacitor between floating ground and ground.

As shown in Figure 7 and Eq.(2-3), the CM noise generated from no well grounding can be obtained.

$$\Delta U_{load} = U'_{load} - U_{load} \tag{4}$$

where, ΔU_{load} expresses the CM noise generated from no well grounding.



(a) CM conducted EMI noises between live/neutral and ground lines



(b) CM noise generated from no well grounding due to parasitic capacitor.

Figure 7. CM noise generated from no well grounding

To solve the above problem, the PCB should be well grounding, especially the DC power supply, such as 5V, 3.3V, 1.8V, 1.2V and so on. In practice, some ferrite beads were used to protect the mutual interference between the above DC power supplies, as shown in Figure 8(a), where $U_1=U_2$, $C_1=C_2=22\mu$ F, $C_3=C_4=C_5=C_6=0.1\mu$ F.



Figure 8. CM noise mitigation method for no well grounding

The high frequency impedance should be considered due to the two ferrite beads. To solve the problems, the two ferrite beads were removed and two capacitors were placed, as shown in Figure 8(b), where $C_7=100$ pF, $C_8=10$ pF. And the high frequency impedance between DC power supplies can be ignored.

5. Experiment & Verification

To verify the proposed methods, the conducted EMI noise generated from the converter is analyzed in the paper. According to the EN 55022, R&S EMI receiver ESL3 and R&S artificial mains network (AMN) ENV216 are used to measure the conducted EMI noise.





Figure 9. Conducted EMI noise experiment and verification for converter

The original conducted EMI noise of the converter is shown in Figure 9(a), and the noise can't pass EN 55022 class B. The Quasi peak (QP) and average value (AV) of the conducted EMI noises are very high. To solve the conducted EMI noise problem, the mitigation approaches are proposed as follows:

1) EMI filter for the converter is designed, as shown in Figure 9(b), where L_1 denotes 10 mH CM choke, both L_2 and L_3 denote 1mH inductance, C₁, C₂, C₃ and C₄ signify 0.033µF, 0.01nF ,10nF and 1nF, respectively.

2) 10nF capacitor is shunt between the source and drain electrodes of the MOSFET.

3) The ground plane is designed for PCB to well grounding.

As shown in Figure 9(c), by employing the above mitigation method, the conducted EMI noise of the converter was decreased significantly and can pass the EN 55022 Class B, which verify the present method effectiveness and validation.

6. Conclusion

In the paper, the measurement uncertainty, noise mechanism and mitigation method for conducted EMI noise are proposed to solve the EMI problem for the PV converter.

1) The uncertainty of the AMN under PV converter side is analyzed due to high frequency parasitic inductance of the interface adapter, which can improve measurement accuracy.

2) A novel NSN is designed to identify the CM and DM noises from the total conducted EMI noises, which can obtain the noise mechanism and its reduction methods.

3) Transistor filtering and well ground methods are proposed to analyze and mitigate the conducted EMI noise generated from the PV converters.

4) The mitigation methods have been used to a certain convert, which can suppress the conducted EMI noise well and pass the EN 55022 Class B standard.

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